True Kelvin CMOS Test Structure to achieve Accurate and Repeatable DC Wafer-Level Measurements for Device Modelling Applications

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***Abstract* — A 6-pad True Kelvin Test Structure for advanced CMOS devices is proposed in this work. It allows test engineers to make very accurate and repeatable wafer-level measurements required for SPICE modelling applications. This design helps to overcome parasitic resistance of the probe holder and probe which is found to be dependent on test temperatures. It also mitigates increase in probe contact resistance due to oxidation of exposed underlying copper on aluminum capped test pads as a result of repeated probing at elevated temperatures. Most important of all, it enables accurate device measurements with minimal probe scrub, essential for 30 micrometers or less test pads, without the need for frequent probe tip cleaning.**

I. Introduction

Device modelling engineers must have the ability to make very precise and repeatable wafer-level DC measurements so that the device SPICE models they extract are highly accurate. Without accurate measurement data, the device model would be invalid even if the SPICE model has a perfect fit with zero error against a set of erroneous measured data. With the reduction of device on-state channel resistance, Rds, shrinking of test pad sizes and copper backend interconnects for advanced CMOS technologies [1-2], it is increasingly challenging to make accurate and repeatable wafer-level device measurements especially at elevated test temperatures [3]. Currently at 30×30µm, most semiconductor companies are now exploring 20×20µm test pads to reduce development costs. SPICE models have to predict device over-temperature behavior over an even wider thermal range from -40°C to 125°C to now, -50°C to 200°C. The same 30×30µm test pads have to be probed repeatedly at different temperatures with difficulties finding fresh metallization for every new measurement.

To make good, low resistive contacts, probes require at least 30µm of probe scrub (60um Z over-travel) on aluminum test pads as shown in Figure 1. As test pads continue to shrink further, probe tips of smaller sizes would need to be used which will increase the contact and probe parasitic resistances. Most test engineers believe that the pad metal oxide formed on the probe tips causes probe contact resistance to increase, and this has to be resolved by frequent probe cleaning. However, another mechanism of pad degradation also plays a significant role increasing the overall parasitic resistance – repeated probing of the same test pads wearing out the aluminum cap layer exposing underlying slotted copper which oxidizes rapidly and extensively at elevated temperatures. This paper proposes a true Kelvin test structure design to consistently deliver accurate and repeatable measurement for CMOS devices. It also highlights and presents the impacts of oxidation of the exposed underlying copper metallization due to repeated probing at high temperatures.

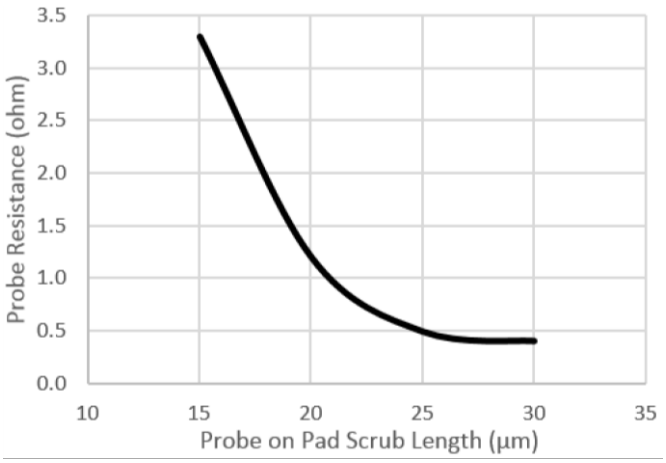

Fig. 1. Typical Probe parasitic resistance versus probe scrub length on Aluminum test pads for DC probe shown in Figure 3.

II. Test Structure Design and Experimental Setup

Figure 2 shows a die photo of CMOS transistors with conventional test structures and true Kelvin test structures designed for this work. Conventional test structures have 4 test pads, accessing the Drain, Gate, Source and Body terminals of the MOSFET. The true Kelvin test structure is designed with 2 more additional sense test pads at the Drain and Source terminals so that semiconductor parametric analyzers such as Keysight's B1500 with Kelvin Force/Sense capability can correct for the parasitic resistances of the cables, probe holder and probes. More importantly, the probe/pad contact resistances as well as the metallization resistances between pad and device terminals are also corrected during measurements. It is vital that the device measured characteristics is not influenced by the metallization between pad and device terminals because SPICE models should only consider the device intrinsic performance and not cater for these metallization parasitic resistances as they are typically only taken into account during post-layout circuit simulations.

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The layout approach for this proposed Kelvin test structure is different compared to those adopted in high current power devices [4]. The Rds of high current power devices are in the milliohm range and these devices are typically very big in size with huge test pads since their device terminals need to handle large currents. Therefore, additional sense test pads are not required because these large test pads are directly above their device terminals and they can accommodate multiple force and sense probe tips. On the contrary, the source and drain of advanced CMOS devices are very much smaller and therefore require the additional sense test pads and metallization to access the drain and source terminals. DC positioners, shown in Figure 3, are used in this work compared to probe card as they offer flexibilities in studying the effects of probe contact resistance on the test pads. NMOS and PMOS devices of various sizes have been fabricated but in this work, results are focused on a W/L=100/0.06µm NMOS device. Keysight B1500 and a Cascade Microtech shielded probe station with thermal chuck are used for the wafer-level measurements.

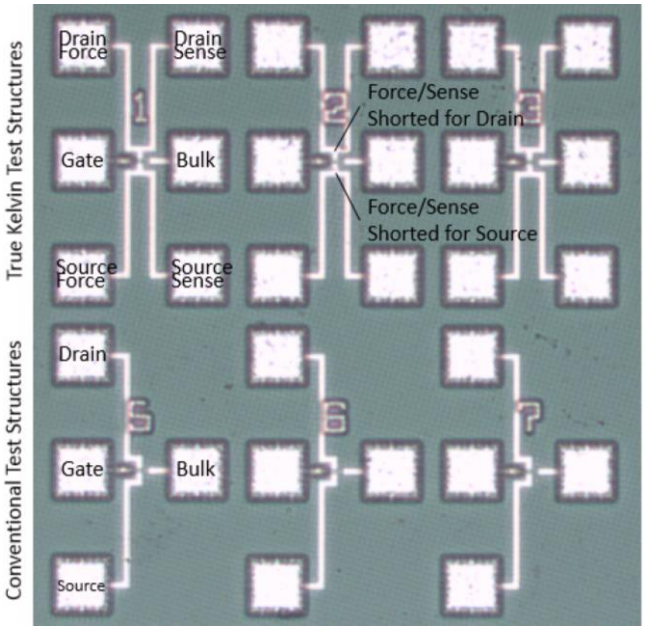


Fig. 2. 4-Pad Conventional versus 6-Pad True Kelvin CMOS Test Structures for Device Modelling.

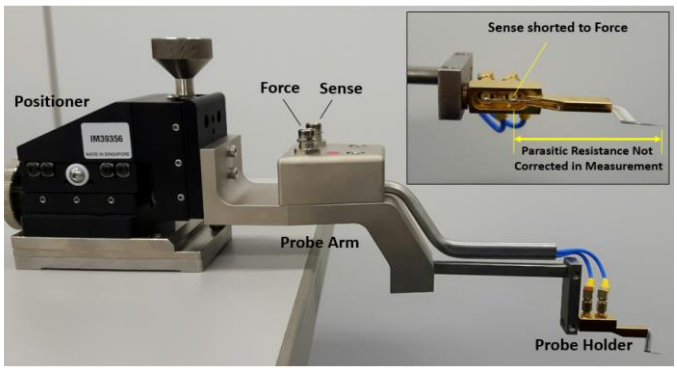


Fig. 3. Typical DC probe for Wafer-Level Device Characterization. Photo inset of the Probe Holder underside showing where the Sense is shorted to the Force and the uncorrected portion of parasitic resistance.

III. Results and Discussions

The parasitic resistances of the probes in contact with the test pads are first characterized. Figure 4 depicts a pair of brand new drain and source tungsten probes (probe tip diameter of 10µm) on a common test pad with 60µm Z over-travel (30µm probe scrub length on test pad). They are probed repeatedly at the same location of this common pad over 100 cycles of chuck in contact-separation positions. At 25°C, it was observed in Figure 4 that the total parasitic resistance for both probes increases from 0.8 to 1.0 ohm in the first 70 contact cycles. Thereafter, the resistance increases to about 20 ohms at 100th contact cycle. This is likely due to the increase pad damage on the test pad which results in larger contact resistance.

Next, the 2 probes were replaced with new ones and they were probed with 30µm scrub length on a new common test pad. The probe parasitic resistance is initially characterized to be about 0.8 ohm to ensure subsequent measurements are properly setup for fair comparisons. The chuck holding the wafer is

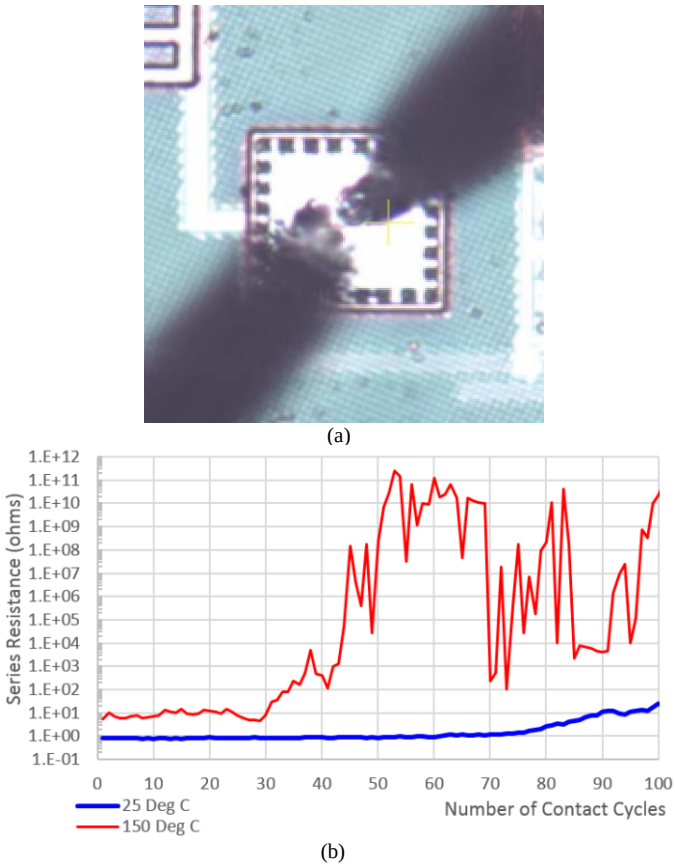


Fig. 4. Die Photo showing measurement of Parasitic Series Resistance of Drain/Source Force Probe Holders and Probes with 2 probes on the same test pad (a) and test results at 25°C and 150°C over 100 Contact Cycles (b).

heated up to 150°C and the same experiment is repeated for 100 contact cycles. In the first 30 contact cycles, the parasitic resistance is about 5 ohms. Reference to Figure 3 suggests that resistance of the probe holder, probe and probe contact resistance is about 0.4 ohm at 25°C and 2.5 ohm at 150°C. If the Rds of CMOS devices continue to reduce with technology scaling, parasitic resistance of the probe holder, probes and probe/pad contact resistance must be corrected to accurately

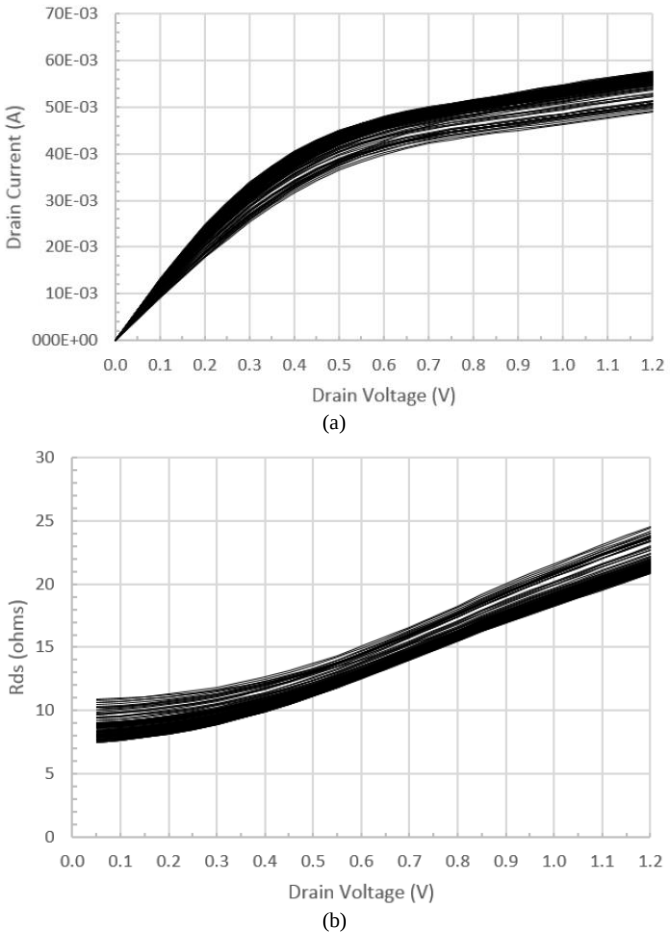


Fig. 5. Id (a) and Rds (b) versus Vd at Vg =1.2V for W/L=100/0.06µm NMOSFET for 4-Pad Conventional Test Structure for 100 Contact Cycles at 25°C.

reflect the intrinsic device performance, particularly at elevated temperatures. This means that, at the very least, the force/sense terminals must be at the test pads to correct for the parasitic resistances in the measurement system. Beyond 30 contact cycles, we observed that the probes are not making any electrical connections with the test pads. From Figure 4, at 150°C, the underlying copper of the Aluminum capped test pads has been exposed by repeated probing and copper oxidation has occurred. As copper oxide is permeable, the oxidation of the underlying copper was so extensive and widespread that the 2 probe tips on the common test pad suffer electrical continuity failures.

With a good baseline characterization of how the 2 probes interact with a single common test pad at 25 and 150°C, NMOS with the size of W/L=100/0.06µm is selected for characterization at 25°C and 150°C. Figure 5 and 6 compares the Id and Rds versus Vd behavior at Vg=1.2V for 4-Pad conventional test structure and 6-Pad true Kelvin test structure over 100 Contact Cycles. The true Kelvin test structure produces very accurate and repeatable test results even when the probes repeatedly scrub on the same spot of the test pads over 100 contact cycles. The proposed test structure is capable of handling and correcting for the increase in measurement system's parasitic resistance from 0.8 to 20 ohms over the 100 contact cycles.

On the contrary, test results for the conventional test structure is not repeatable and therefore unacceptable. Figure 7 is extracted from Figure 5 and 6 with Id and Rds at Vg=1.2V, Vd=0.6V as well as Vg=1.2V, Vd=1.2V, plotted against the 100 contact cycles. It is observed that when true Kelvin test structure is used, the Id is much larger, by about 10 to 25% for both Vd at

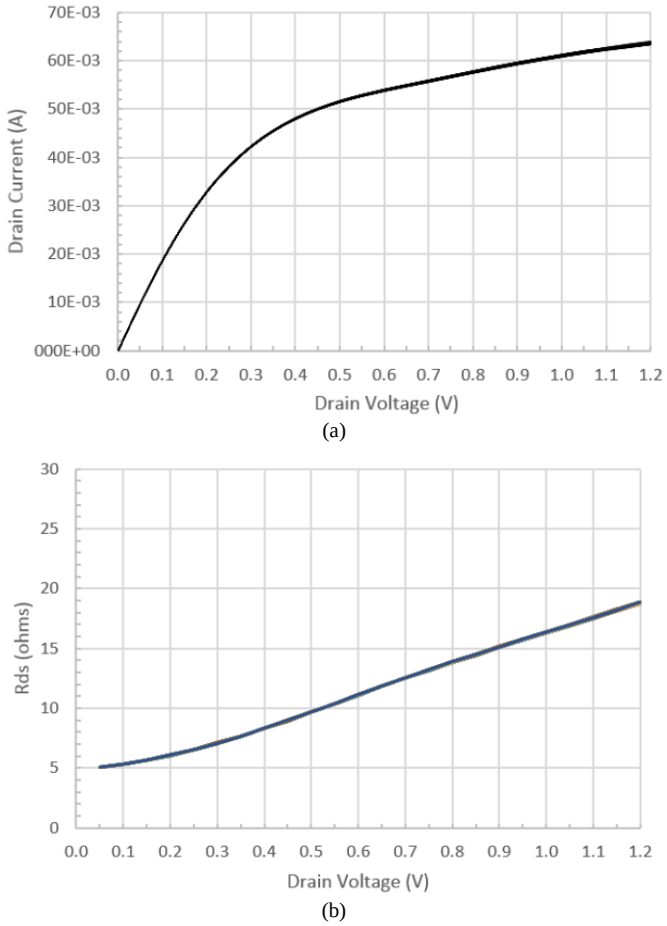


Fig. 6. Id (a) and Rds (b) versus Vd at Vg =1.2V for W/L=100/0.06µm NMOSFET for 6-Pad True Kelvin Test Structure for 100 Contact Cycles at 25°C.

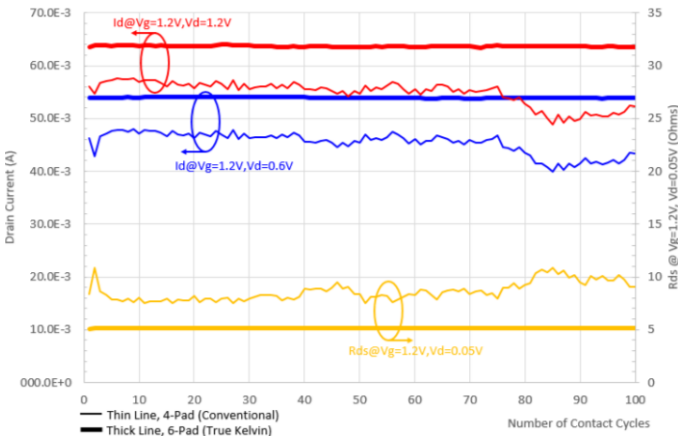
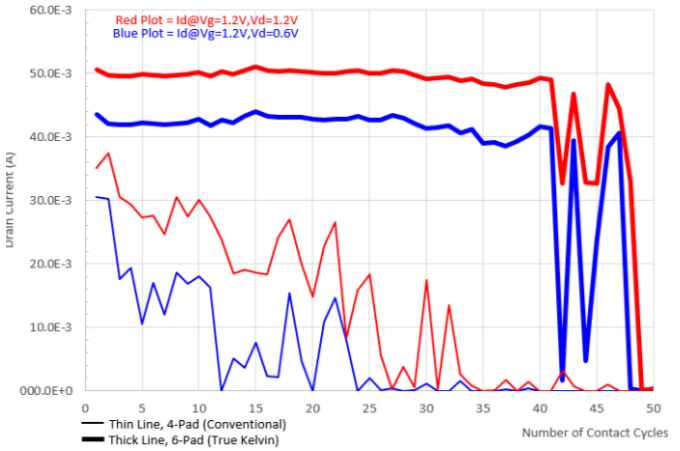


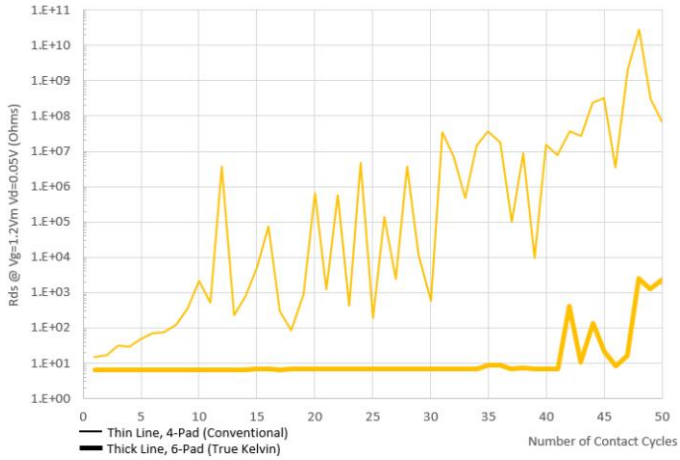
Fig. 7. Id and Rds versus Contact Cycles for W/L=100/0.06µm NMOSFET for 4-Pad Conventional Test Structure and 6-Pad True Kelvin Test Structure at 25°C.

0.6V and 1.2V. The conventional test structure results in much larger device Rds measured compared to the true Kelvin test structure by more than 50 to 110% because the parasitic resistances of the probe, probe holder as well as metallization between pad and device are not corrected.

The NMOS device measurements is repeated at 150°C with new probe tips on a new device and the test results are presented in Figure 8. Generally, much larger Id and smaller Rds are again



(a)



(b)

Fig. 8. Id (a) and Rds (b) versus Contact Cycles for W/L=100/0.06µm NMOSFET for 4-Pad Conventional Test Structure and 6-Pad True Kelvin Test Structure at 150°C.

observed for the true Kelvin test structure. In the first contact cycle, Id is larger by 30% and Rds is smaller by about 130% when comparing true Kelvin to conventional test structure. Interestingly, at the 43rd contact cycle, the Force/Sense Kelvin correction capability of B1500 (High Resolution SMU, 50mA, 40V at 2W power rating) failed due to too large contact resistance as a result of oxidation of underlying copper beneath the aluminum capped test pads. This observation correlates very well with Figure 4 where it is also noted that at 150°C, the total resistance of 2 probes on the same pad increases beyond 1 kOhm at around the 40th contact cycle.

IV. Conclusions

The 6-pad true Kelvin test structure proposed in this work allows device engineers to make very accurate and repeatable wafer-level device measurements required for SPICE models. It successfully overcomes the parasitic resistances of the probe holder and probe which increase with temperatures. The test structure also copes well with the oxidation of exposed copper underneath the Aluminum capped test pads at elevated temperatures. Although such an approach consumes more layout space, with Rds decreasing in technology scaling and reduction of test pad sizes to less than 30µm, making accurate wafer-level measurements repeatedly on the same device at various different temperatures is becoming even more challenging, especially when smaller pads are unable to accommodate probe scrub of 30µm or more. The proposed test structure outlined in this research paper is robust and insensitive to probe parasitic resistance, probe/pad contact resistance, probe scrub length on the pads as well as the frequency of probe tip cleaning. It has succeeded in making accurate, reliable and repeatable wafer-level device measurements for device modeling applications.

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