



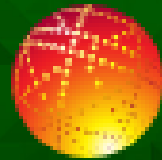
**SWTEST**

PROBE TODAY, FOR TOMORROW

# **Silicon Photonics - Challenges & Solutions for Wafer-Level Production Tests**



**Dr Choon Beng Sia**



**GLOBALFOUNDRIES**

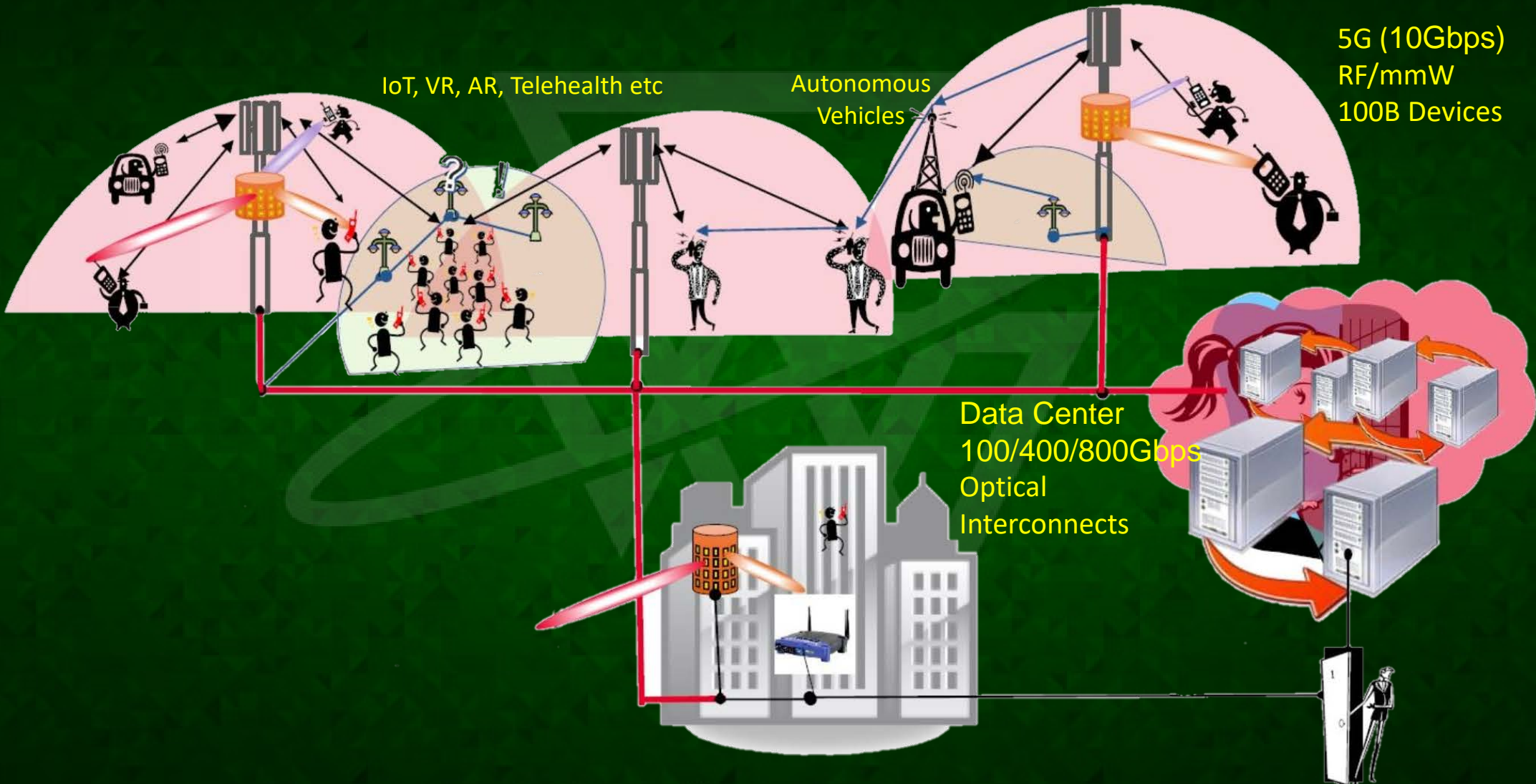
**Dr Johnny Yap,  
Ashesh Sasidharan, Robin Chen,  
Soon Leng Tan, Guo Chang Man**

June 2-5, 2019

# Overview

- **Why Huge Demands for Silicon Photonics?**
- **Why Wafer-Level Photonics Tests?**
- **What are the Photonics Test Challenges & Possible Solutions?**
  1. How to Optimize Test Setup for Accurate & Repeatable Measurements?
    - How to couple light into a photonics chip (wafer-level)?
    - Optimizing Fiber Height and Incident Angle.
  2. How to Correlate Wafer-Level Test to Final Product test?
  3. How to Achieve Fully Automatic Wafer-Level Production Solution?
- **Summary**

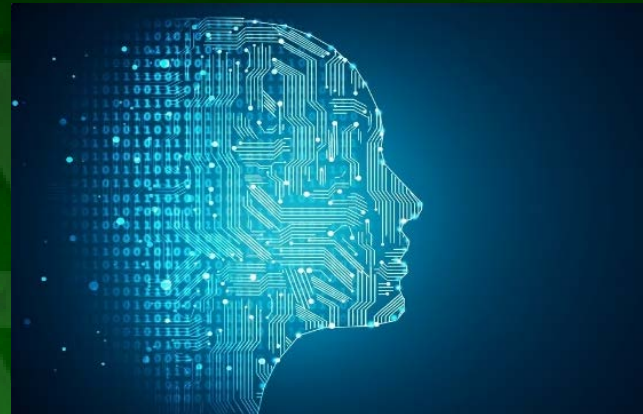
# Communication Network for 4<sup>th</sup> Industrial Revolution



# The Need for High Performance Network & Data Centers



Big Data Analytics



Artificial Intelligence



Genomics Revolution



Financial Acceleration



Cyber Security



Video Transcoding

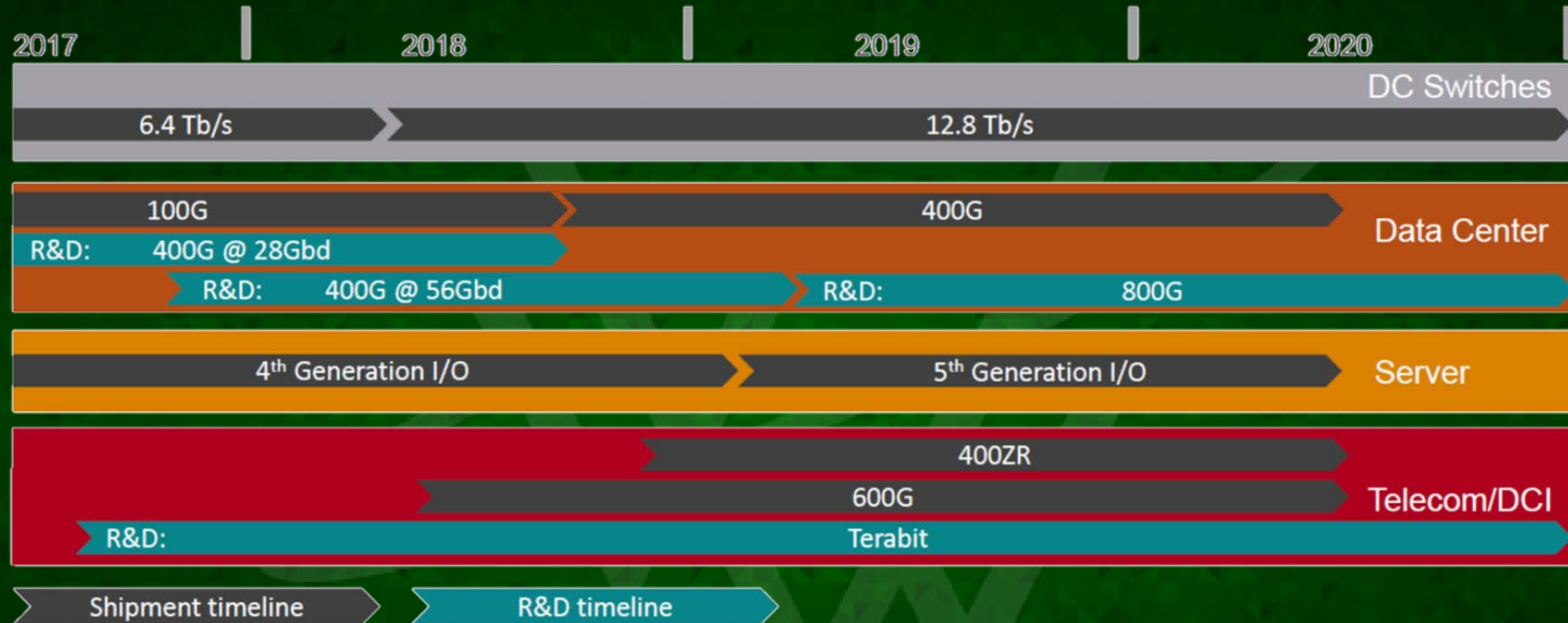
# Facebook Invests US\$1B HyperScale Data Center in Singapore

- **Facebook's 1<sup>st</sup> Data Center in Asia (Hub).**
  - IT Talent & Fiber connectivity
  - 170,000 m<sup>2</sup>
  - 150MW
- **5000 servers**
  - Each server supports 100 petabytes or 100,000 TB\*



Artist Impression of Facebook Data Center in Singapore

# Requirements for Data Center – High Speed Data Rate



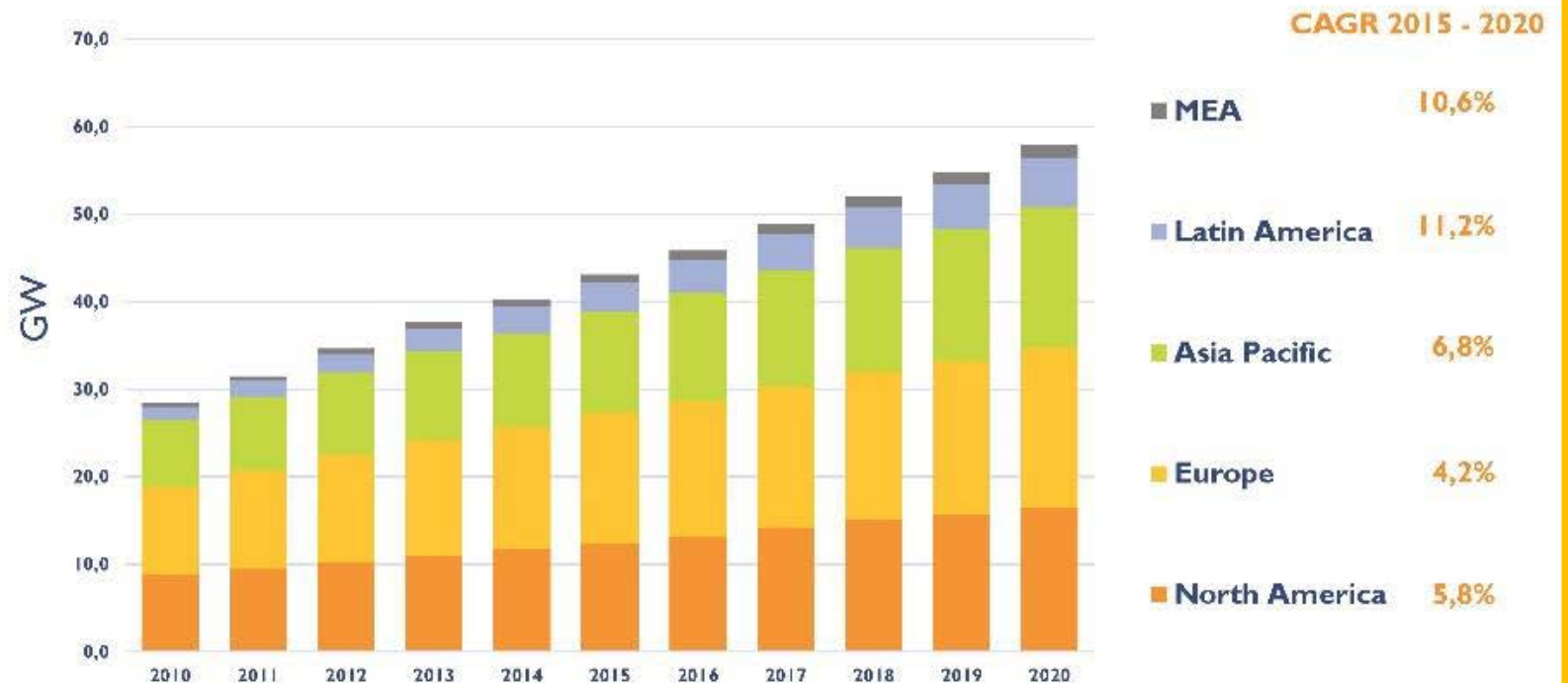
- **Wired communication network.**
  - High Speed, High Data Rate, Low Latency requirements.

# Requirements for Data Center – Energy Efficiency

- **Biggest challenge – Not Speed but Reducing power consumption!**
- **Power Usage**
  - 40% - Server & Switch
  - 40% - Cooling
- **Today, Data Centers consume ≈7% of Earth's power**
- **\*By 2025, 20%?**

## WORLDWIDE DATA CENTER FACILITIES – POWER NEEDS IN GW

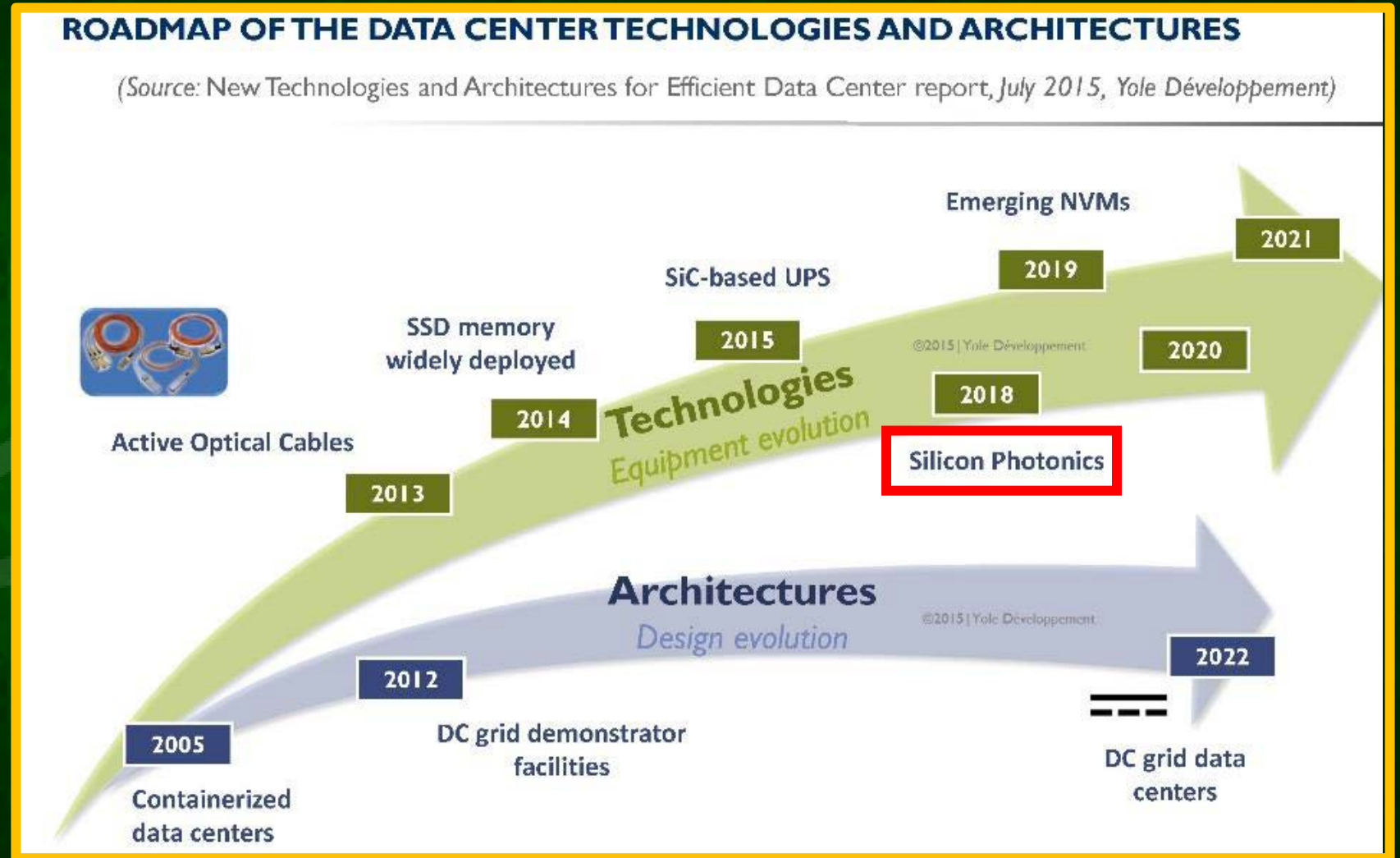
(Source: New Technologies and Architectures for Efficient Data Center report, July 2015, Yole Développement)



**With no slowdown in new facility construction, data centers worldwide will have an increasing need for power.**

# Requirements for Data Center – Energy Efficiency

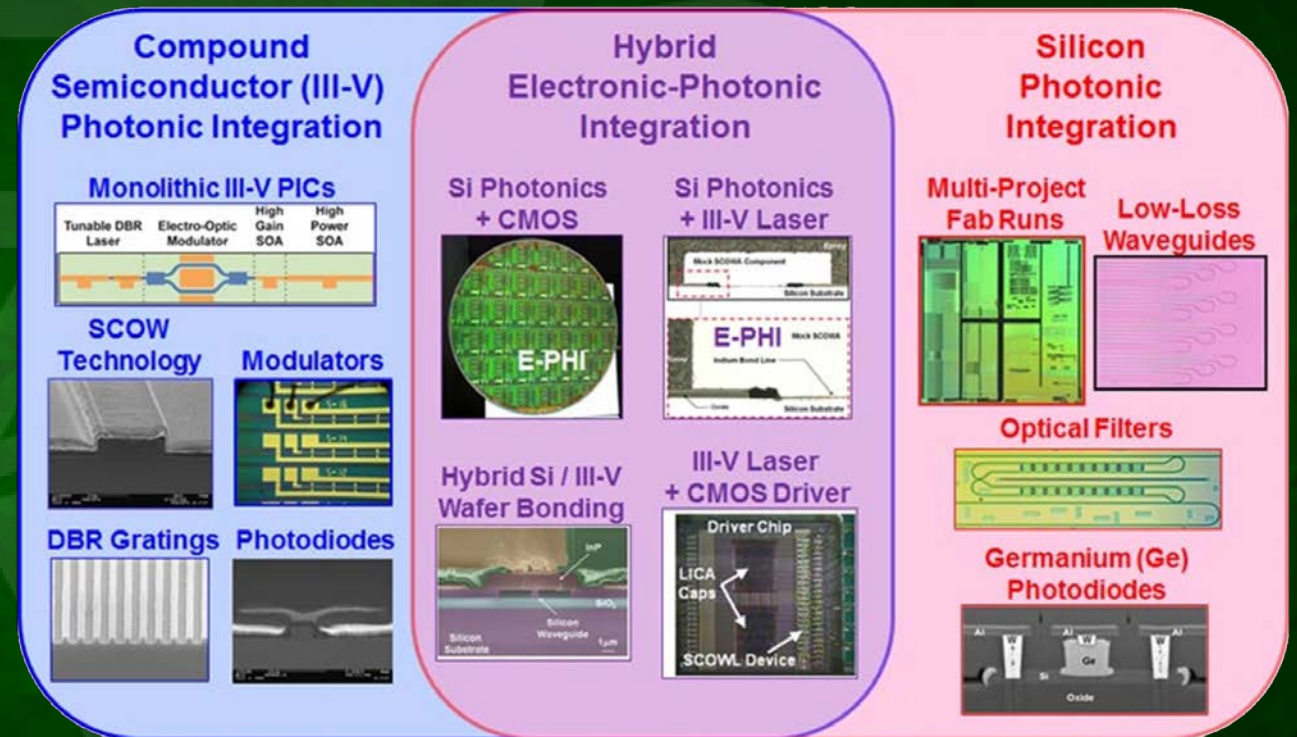
- Urgent need for Energy-Efficient Data Centers
- SiPh technology is rising star in high speed data transfer.





# Why Silicon Photonics?

- **Improvements in Thin Film Growth**
  - High Quality Ge on Si
    - Excellent Lattice Matching
    - Hi-Speed Ge-on-Si Photodiodes
- **Exploiting Silicon Technologies**
  - Low-Cost High-Volume Production
  - Low-Power Logic devices
  - High-Speed RFCMOS devices
  - Heterogenous Integration/Packaging



# SiPh Optical Transceivers for Data Centers

## Components on SiPh Transceivers

### 1. CMOS Logic Chip

- Data Encoding (also decoding)

### 2. Optical Transmitter

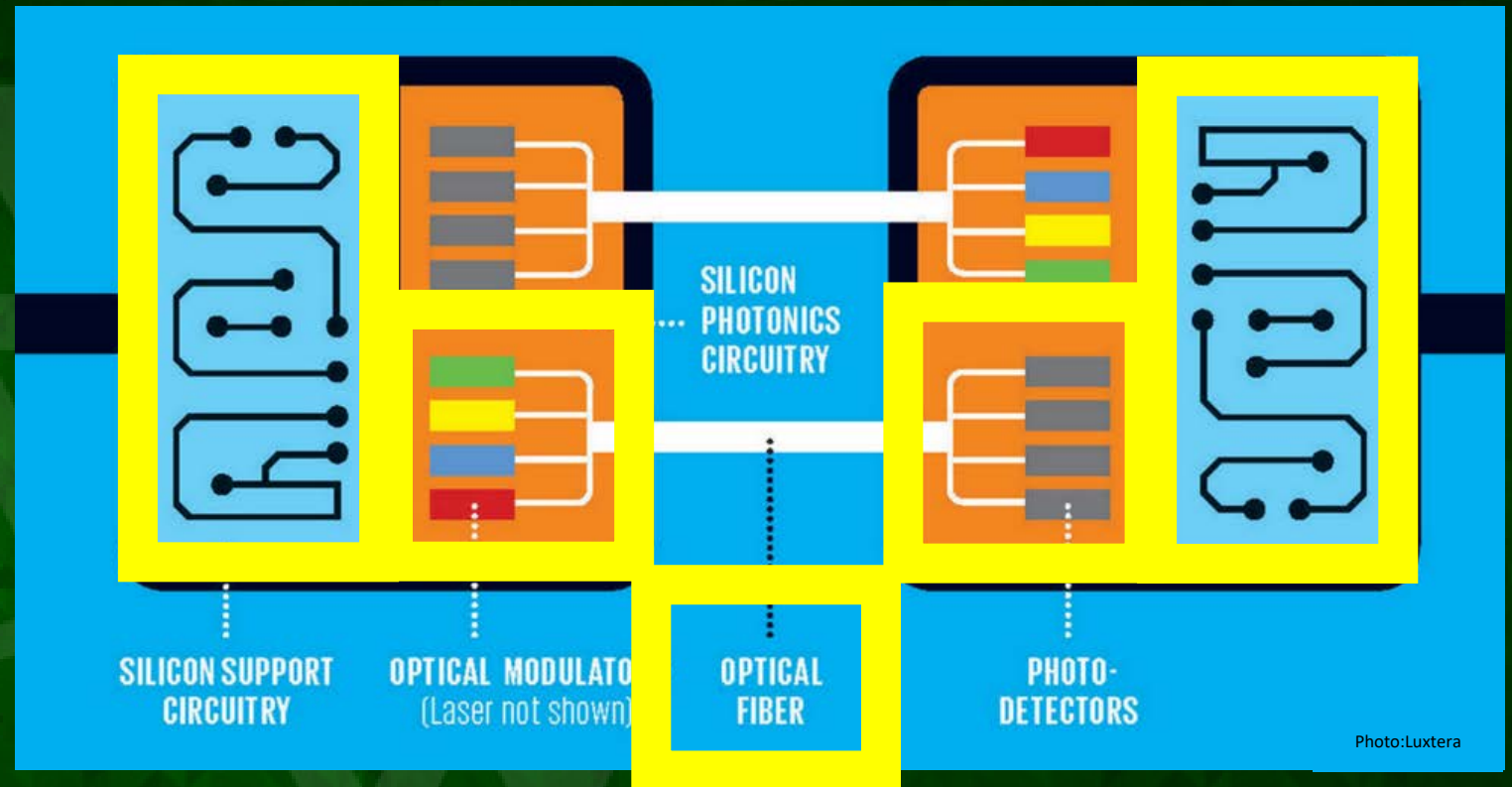
- Optical Modulators - Varying voltage modulate Data onto Light
- Lasers not implemented on Silicon

### 3. Optical Receiver

- Ge Photo detectors
- Converts Light to Voltage

### 4. CMOS Logic Chip

- Data Decoding (also encoding)



For a 10Gb/s Link	Copper Interconnect	Optical Fiber
Power Required	10 W	0.2 W
Range	meters	kilometers

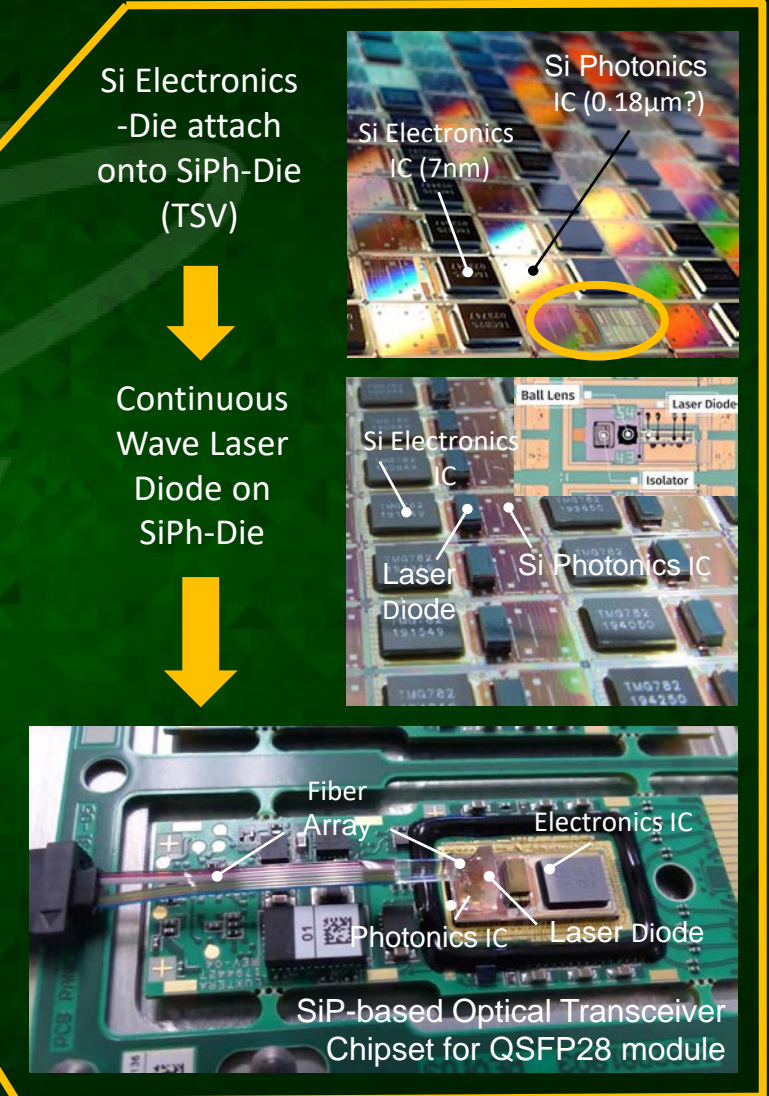
# Evolution of Optical Transceivers



CFP	CFP2	CFP4	QSFP28
4 Ports/Chassis	8-10 Ports/Chassis	16-18 Ports/Chassis	18-20 Ports/Chassis
24W	8W	5W	3.5W

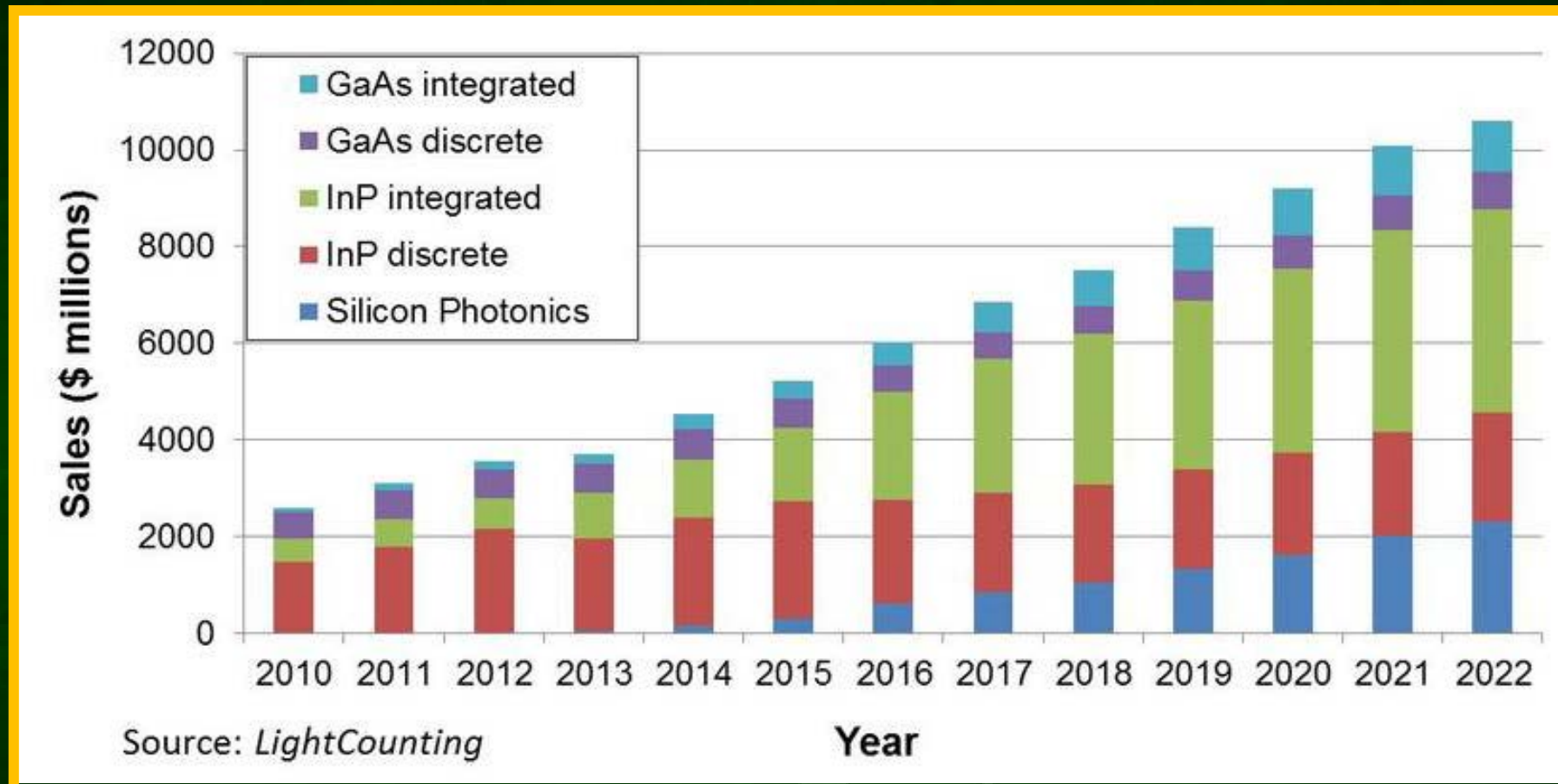
Time

# Why Wafer-level Tests?



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# Integrated Optical Transceiver Market



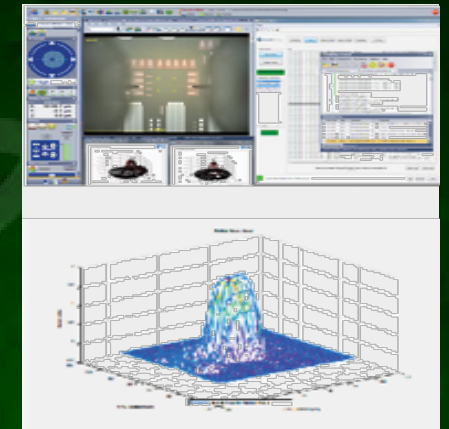
SiPh  
US\$2.3B  
(US\$1.6B)

- **SiPh Transceivers - US\$2.3B, CAGR >35% (2022).**
- **Demonstrate using SiPh in Switches for Data Centers.**

# Integrated Wafer-Level Photonics Test Solution



Optical Test Instruments & Software



Software for Optical Positioners & Probe System



6-Axis/Piezoelectric Positioner, Single Fiber/Fiber Array, Displacement Sensors



RF probes, ISS, Cal. Software & DC probes

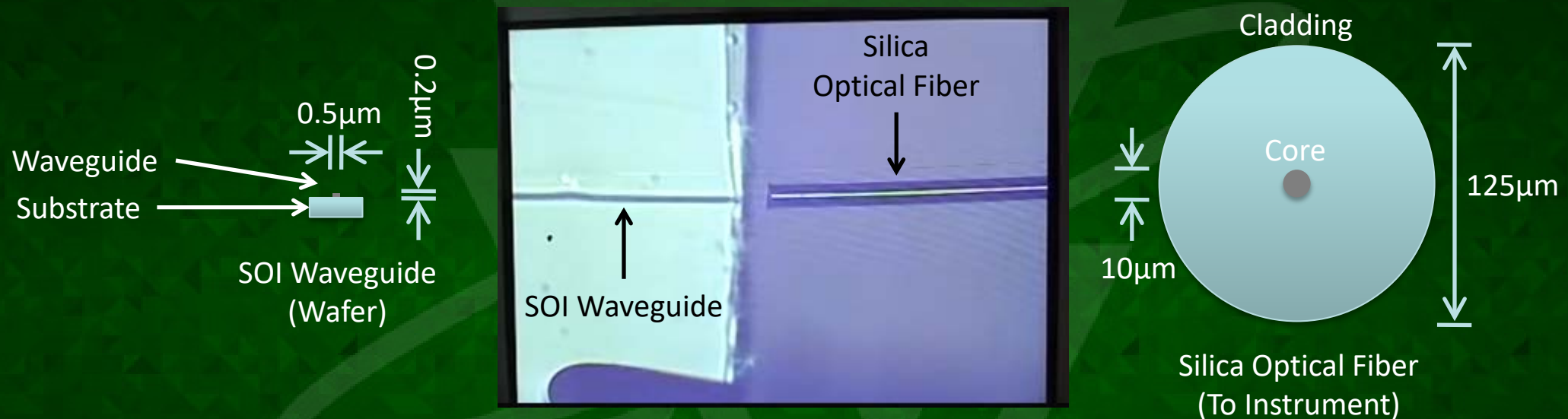


Fully Automatic Probe System with Wafer Loader

# Overview

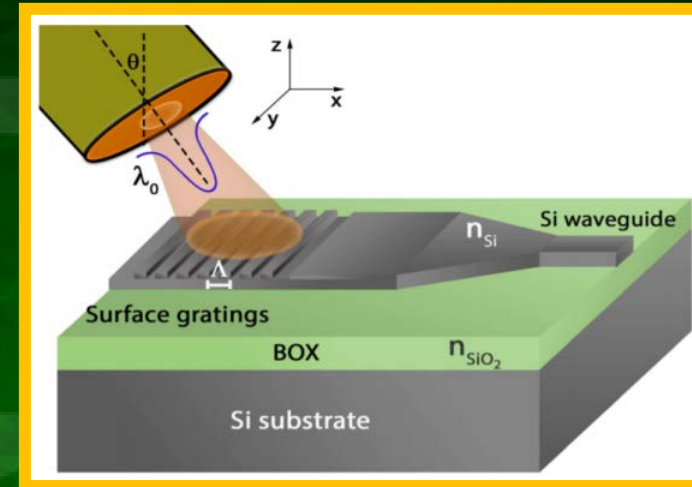
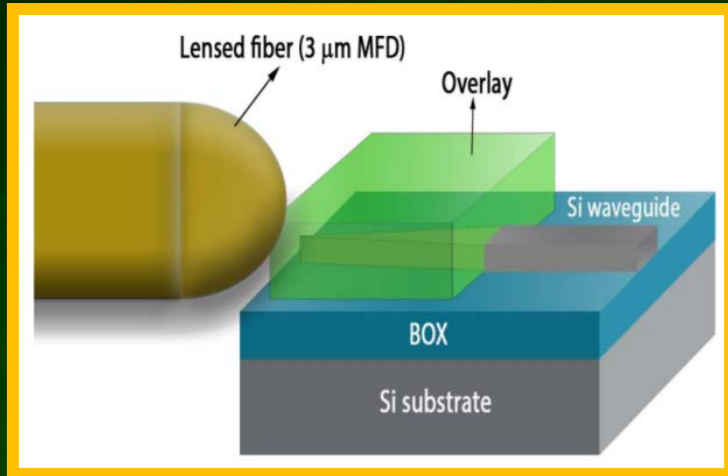
- Why Huge Demands for Silicon Photonics?
- Why Wafer-Level Photonics Tests?
- **What are the Photonics Test Challenges & Possible Solutions?**
  1. How to Optimize Test Setup for Accurate & Repeatable Measurements?
    - How to couple light into a photonics chip (wafer-level)?
    - Optimizing Fiber Height and Incident Angle.
  2. How to correlate wafer level test to final product test?
  3. How to Achieve Fully Automatic Wafer-Level Production Solution?
- **Summary**

# 1.1. How to Couple Light into a Photonics Chip (Wafer-level)?



- **Fiber vs SOI Waveguide – 2 order mag difference in Size**
- **Direct Coupling  $\approx$  >96% Insertion Loss\***

# 1.1. How to Couple Light into a Photonics Chip (Wafer-level)?



- **Edge Coupling**

- Final Product (Die Level)
- Sub-dB Loss Per Facet
- 200nm – 300nm Bandwidth
- Low Polarization Sensitivity
- Harder to Fabricate/Test
- Fixed Interface (Edge of Chip)
- Low Fiber-Chip Alignment Tolerance

- **Grating Coupling**

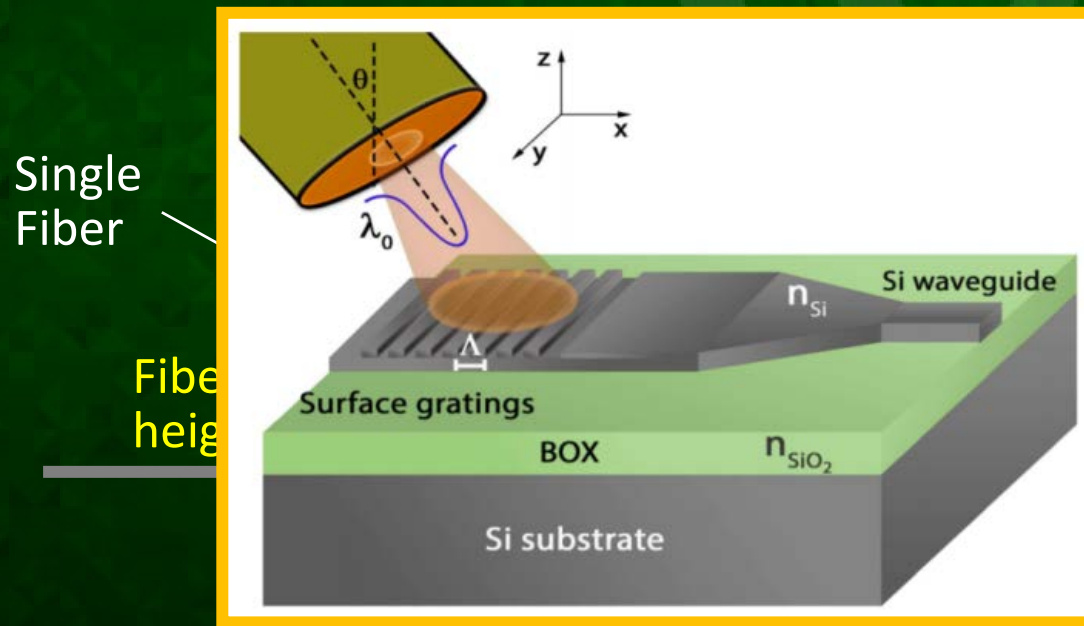
- Process Development & KGD (Wfr Level)
- -2dB → -4dB Loss per Grating Coupler
- Typically 60nm Bandwidth
- Polarization Dependent
- Easier to Fabricate/Test
- Flexibility of interface positions
- High Fiber-Chip Alignment Tolerance



# 1.2. Optimizing Setup – Optical Coupling for Photonics Tests

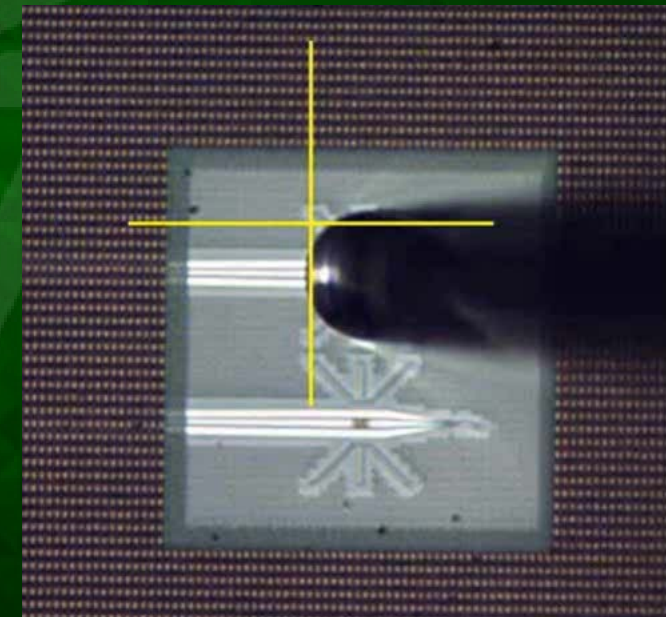
- **Grating Couplers (Wafer-Level Tests)**

- Fast & Repeatable Fiber to Grating Coupler Alignment is available today.
- Fiber Height (Constant Height to Prevent Damage)
- Incident Angle (Critical to determine Optimal Incident Angle before Production Tests)



on wafer

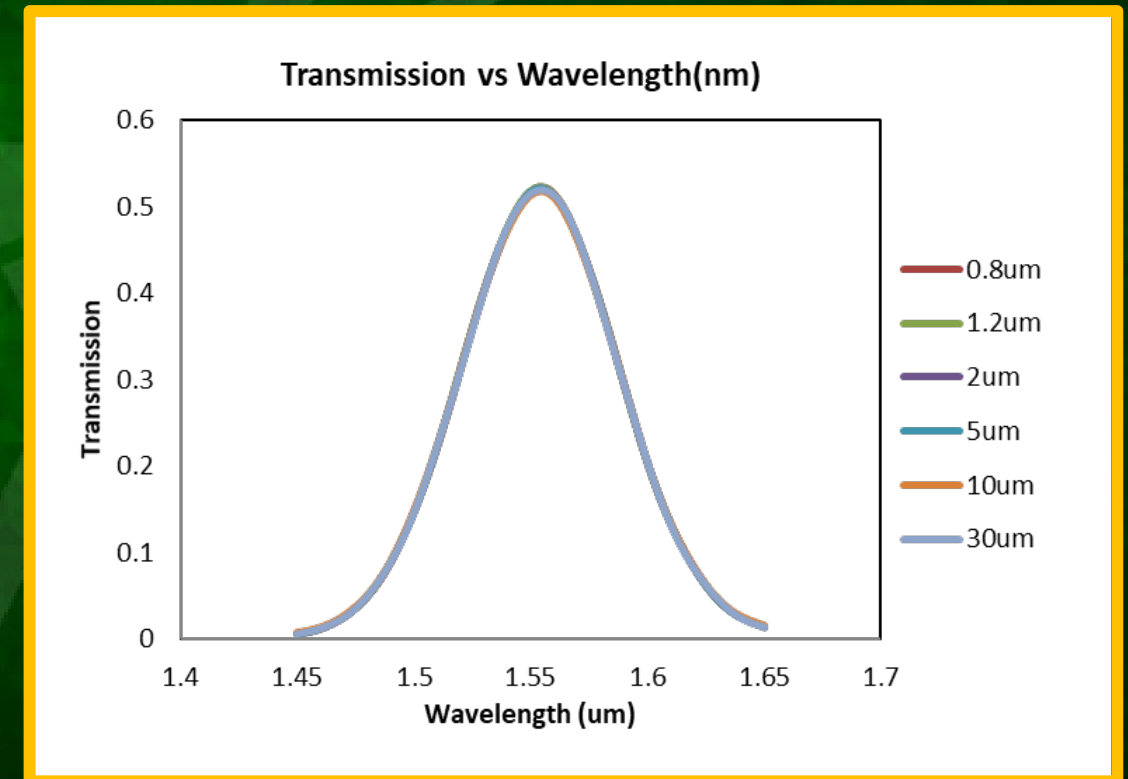
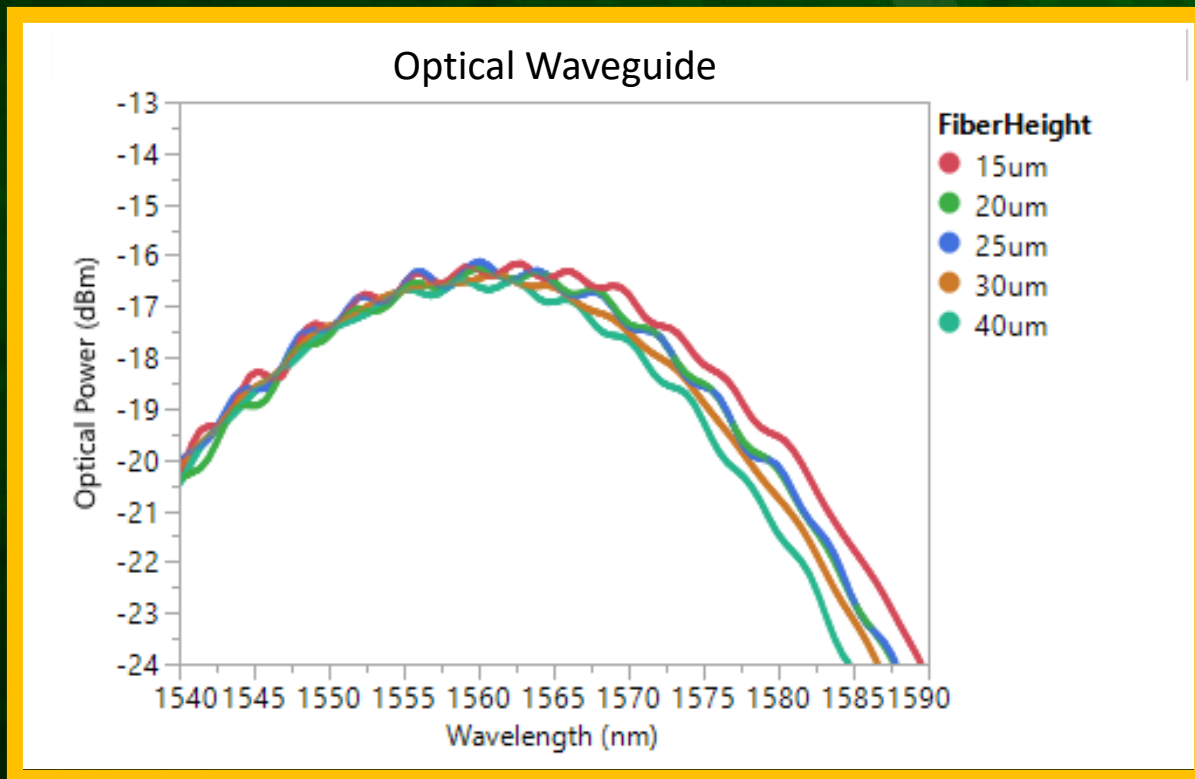
with angle  
incident sensor



Fiber Alignment with Sinusoidal Scan

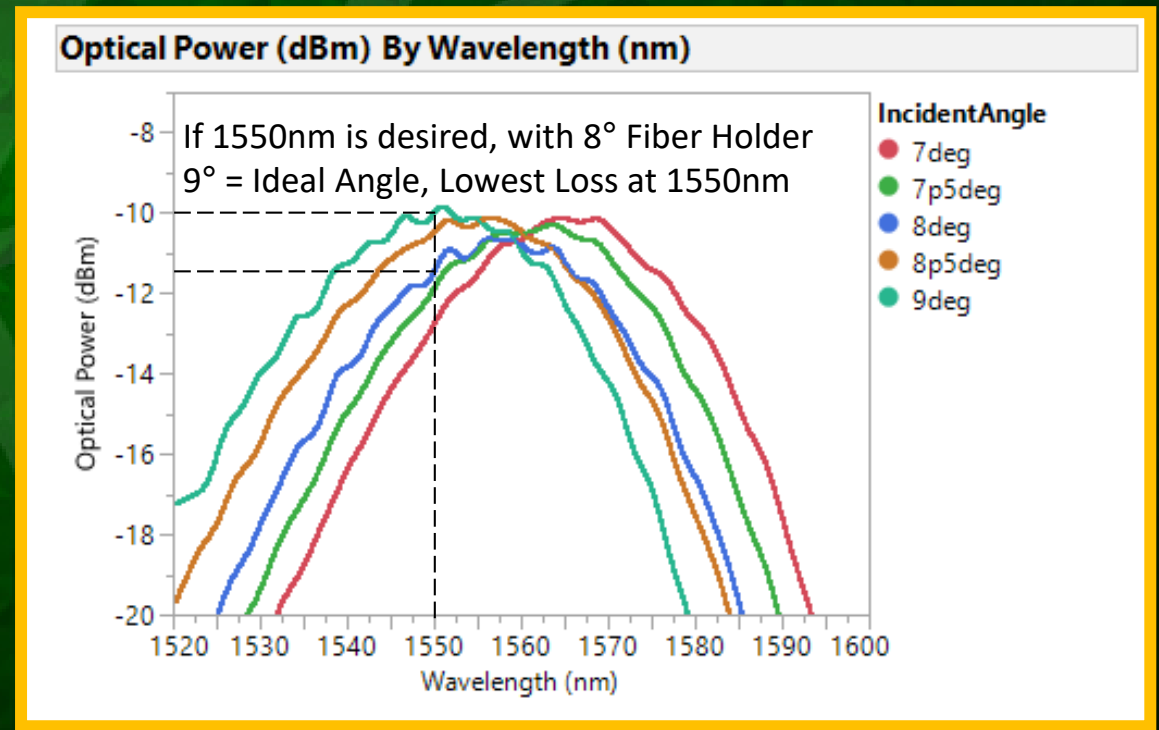
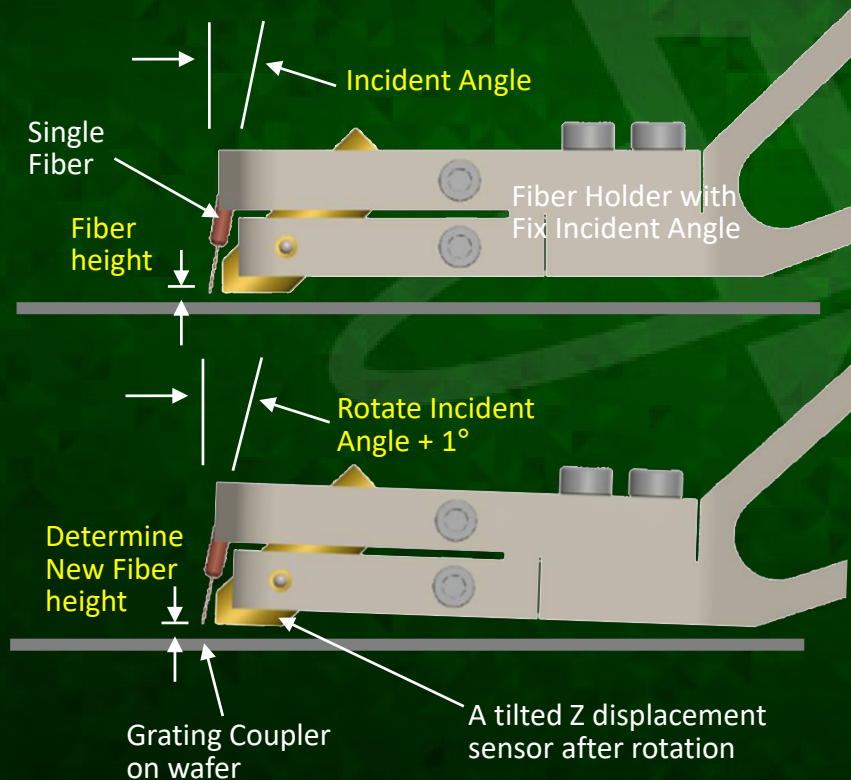
## 1.2.1. Optimizing Setup – Fiber Height (Wafer-Level)

- 1. Set Fiber Height, 2. Peak Search, 3. Make Measurements → Repeat diff. Height
- No Significant Effect on Coupling Efficiency, Peak Wavelength & Bandwidth.
- Good Agreement with Simulation Data.



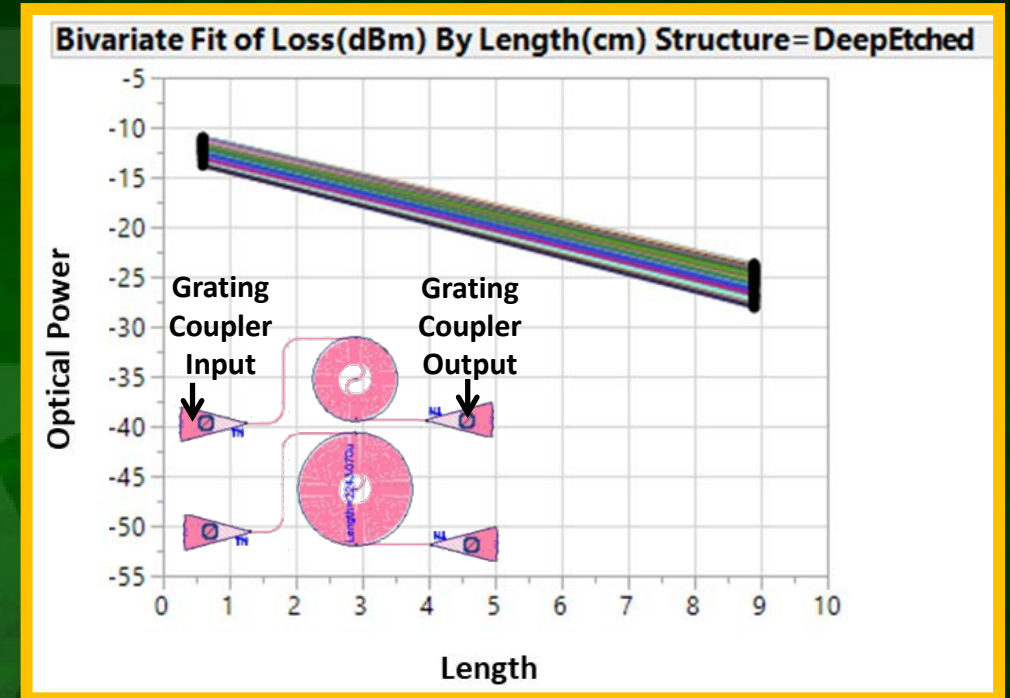
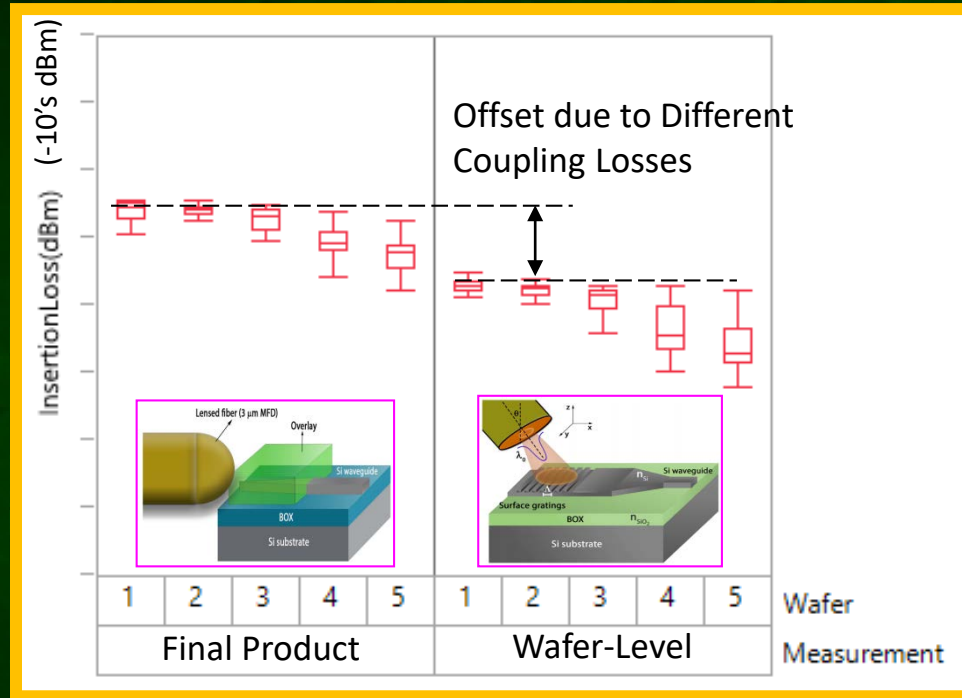
## 1.2.2. Optimizing Setup – Incident Angle (Wafer-Level)

- 1. Set Incident Angle, 2. Peak Search, 3. Make Measurements → Repeat diff. Angle
  - Use 6-axis positioner to vary incident angle  $\pm 1^\circ$  ; Fiber height set with Z sensor (Pivot Cal needed).
- Critical to determine Optimal Incident Angle before Production Tests (1.5dB improvement).



## 2. Wafer-Level vs Final Product Tests (Passive Device)

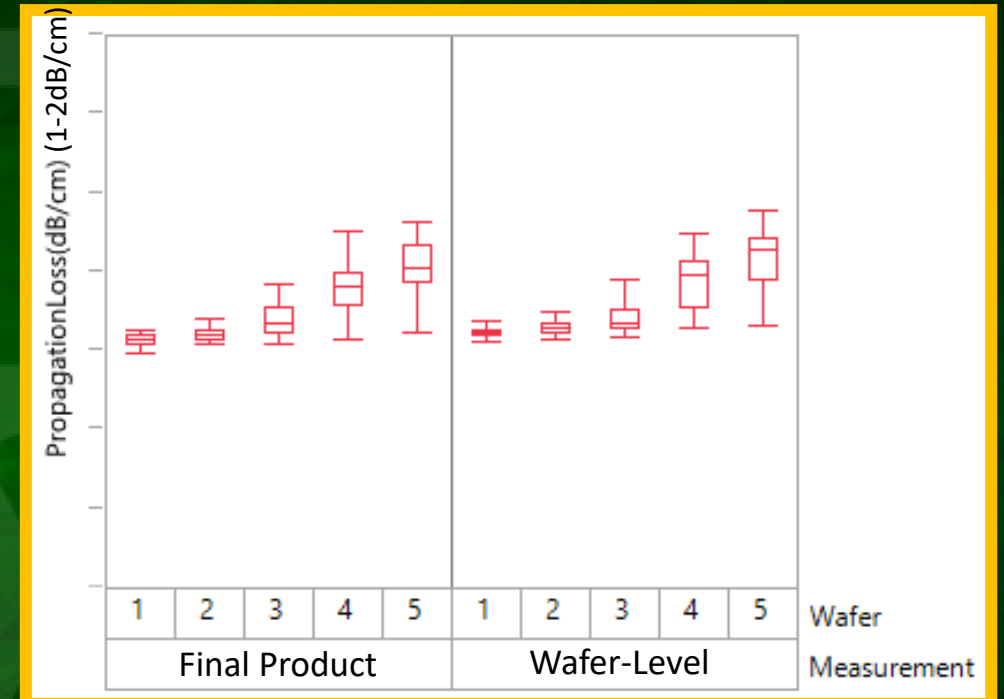
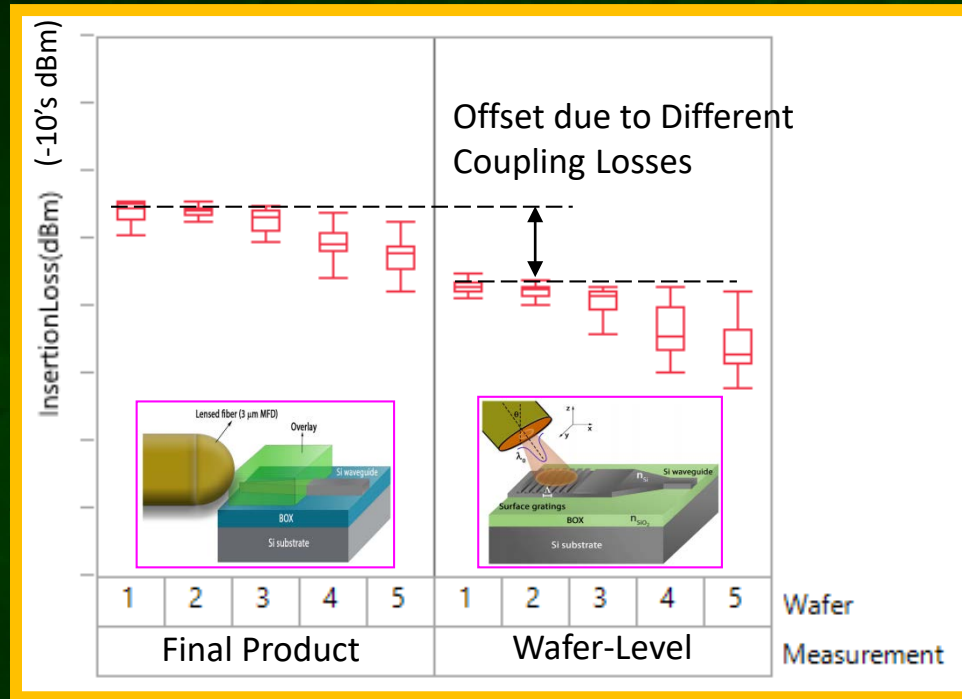
### Offset bet wfr-level & final product      Obtaining Coupling Losses



- Critical to correlate Wafer-Level & Final product Tests
- Using Optical Waveguides as Test Structures
  - Different Insertion Losses observed
- Edge Coupling & Grating Coupling losses are obtained by Cut Back method.
  - Comparing output intensity of waveguides with different length

## 2. Wafer-Level vs Final Product Tests (Passive Device)

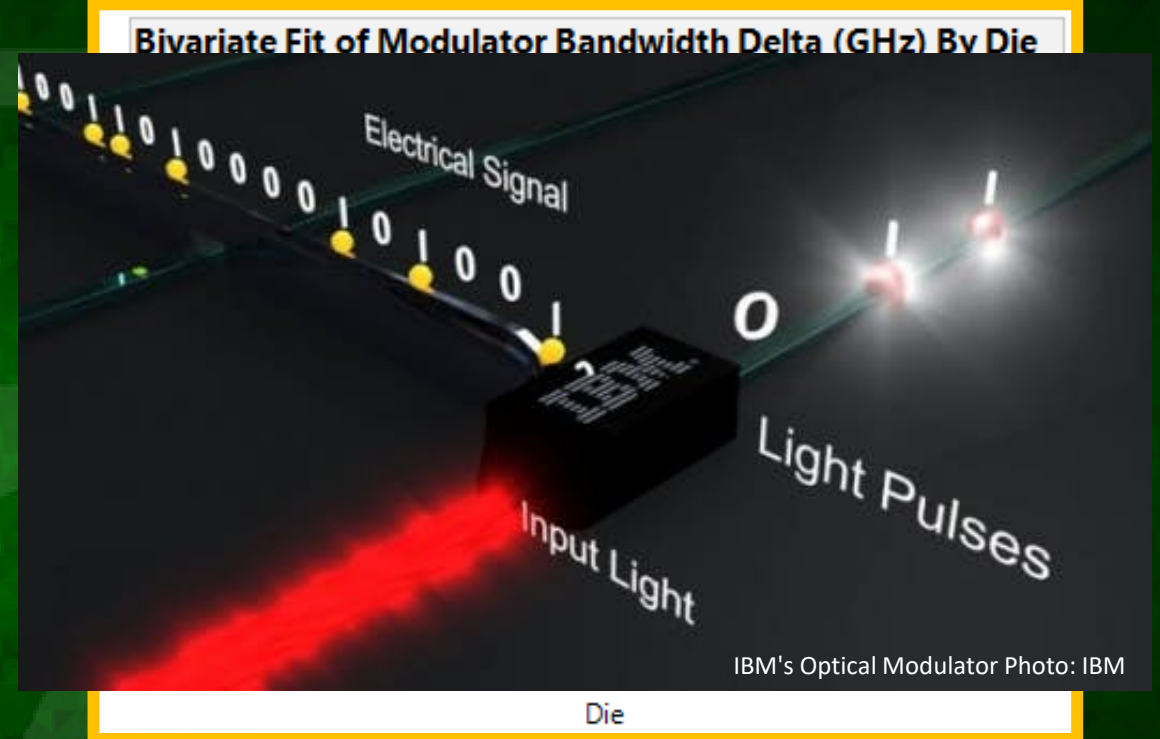
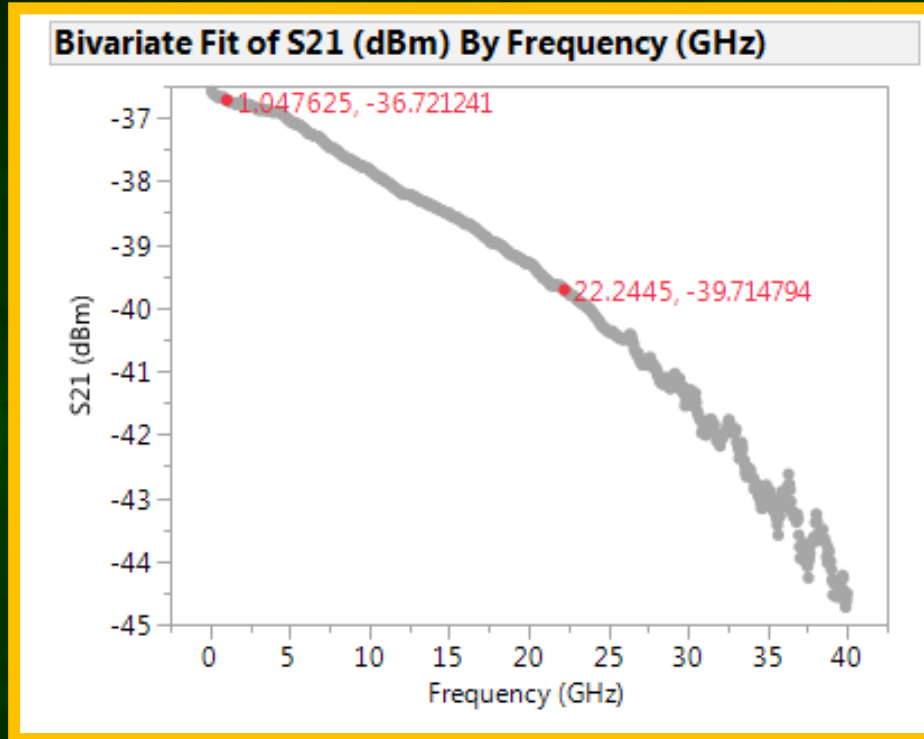
Offset bet wfr-level & final product      After Coupling Losses Correction



- Critical to correlate Wafer-Level & Final product Tests
- Using Optical Waveguides as Test Structures
  - Different Insertion Losses observed

- Remove Coupling Loss
- Comparable Propagation Loss per unit Length.
- Establish Good Correlations between Wfr-level and Final product Tests!

## 2. Wafer-Level vs Final Product Tests (Active Device)



- Testing Optical Modulator (E-O)
- Measure 3 dB Bandwidth for all Dies through Grating Couplers.

- Small Difference in BW for Same Die
- **Good Correlations between Wfr-level & Final Product Tests.**

# 3. Achieving Automatic Production Photonics Tests

- Challenging for one Test Setup to handle...

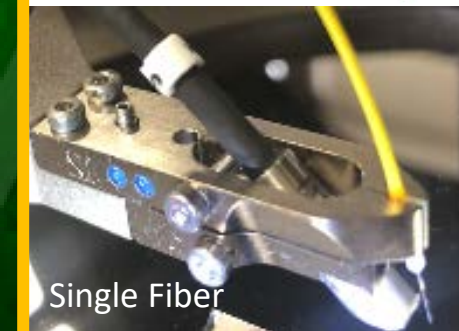
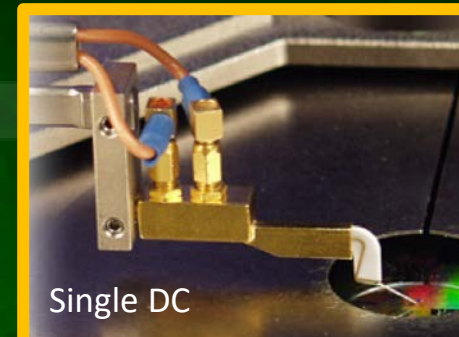
- Passive vs Active Device
- Single Photonics Device & Complex Photonics Integrated Circuit Tests
- Endless Permutations of Test Layouts

- Establish Design Rules, Standardize Layout

(Design for Testability)

- Implement Automatic Testing Architecture

Parameter	Unit	Probes Needed
Photodiode Dark Current	nA	DC probes
N/P-doped Modulator Resistance	ohm	
Heater Resistance	ohm	
Waveguide Propagation Loss	dB/cm	Optical Fiber Probes
Y-splitter splitting ratio	%	
Tap Coupler Coupling Strength	%	
Modulator Extinction Ratio	dB	Optical Fiber Probe(s) + DC Probes
Photodiode Responsivity	A/W	
Modulator Bandwidth	GHz	Optical Fiber Probe(s) + RF Probes
Photodiode Bandwidth	GHz	



Photonics Device Tests

Photonics IC Tests

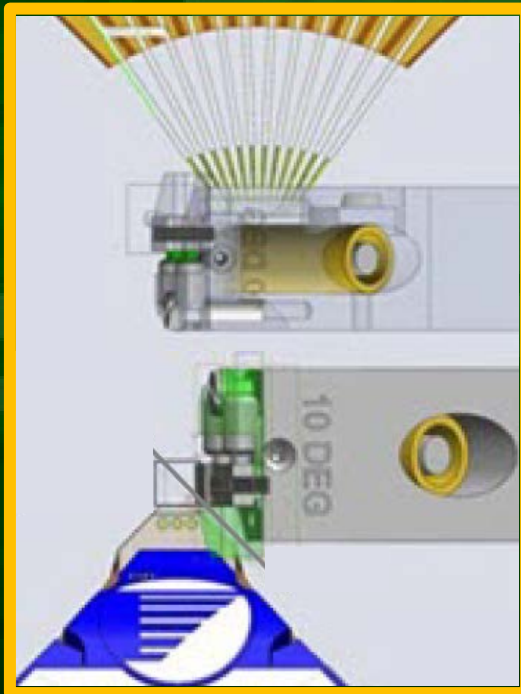
# 3. Achieving Automatic Production Photonics Tests

- **Layout Design Rules & I/O Standardization**

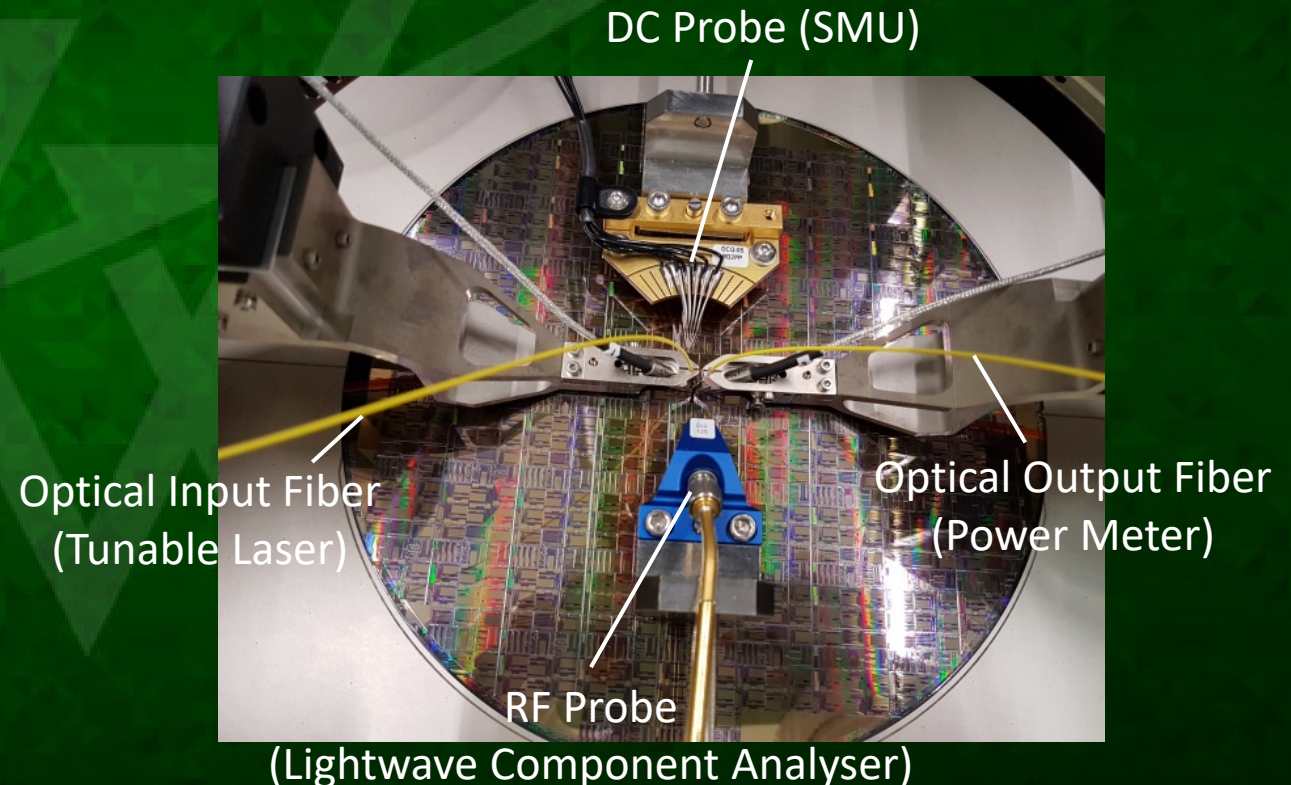
- Establish Test Pads vs Grating Couplers Layout Design Rules.
- Fix DC @North, RF @South, Optical I/Os @East&West side of the DUT.



Design Rules for Single Fiber



Design Rules for Fiber Array



DC Probe (SMU)

Optical Input Fiber (Tunable Laser)

Optical Output Fiber (Power Meter)

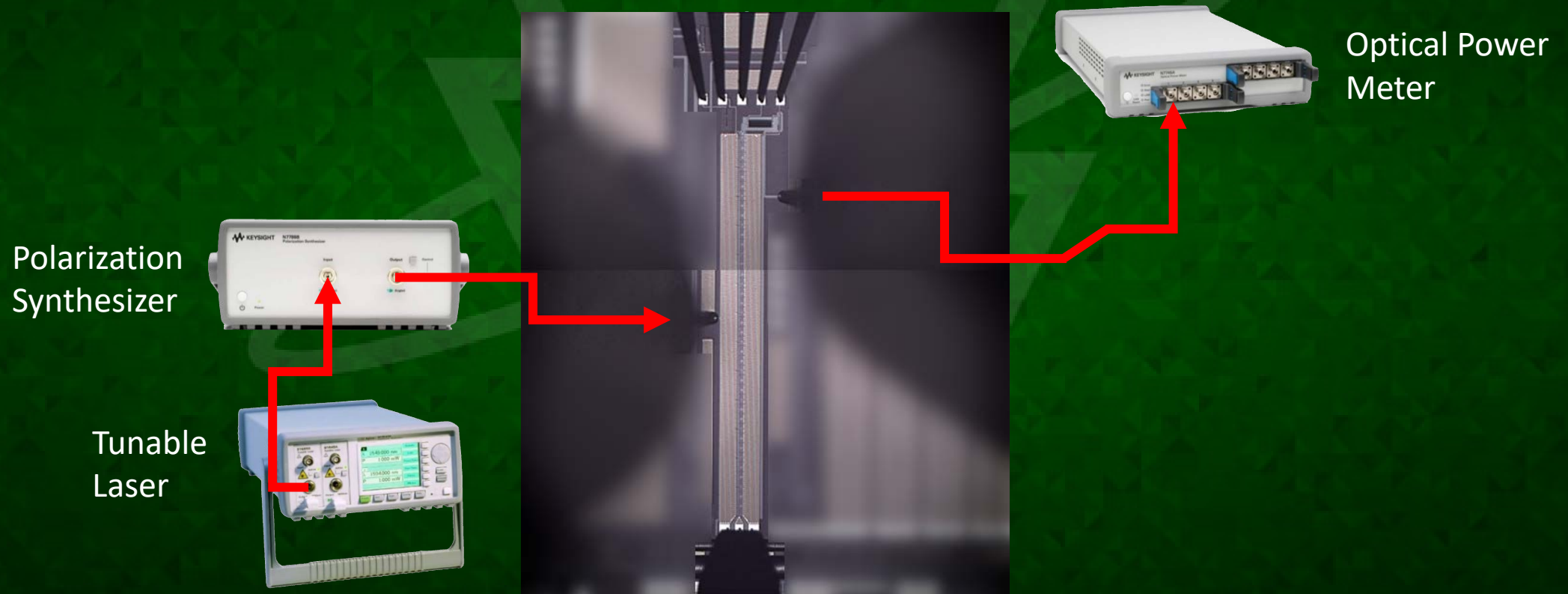
RF Probe

(Lightwave Component Analyser)



# 3. Achieving Automatic Production Photonics Tests

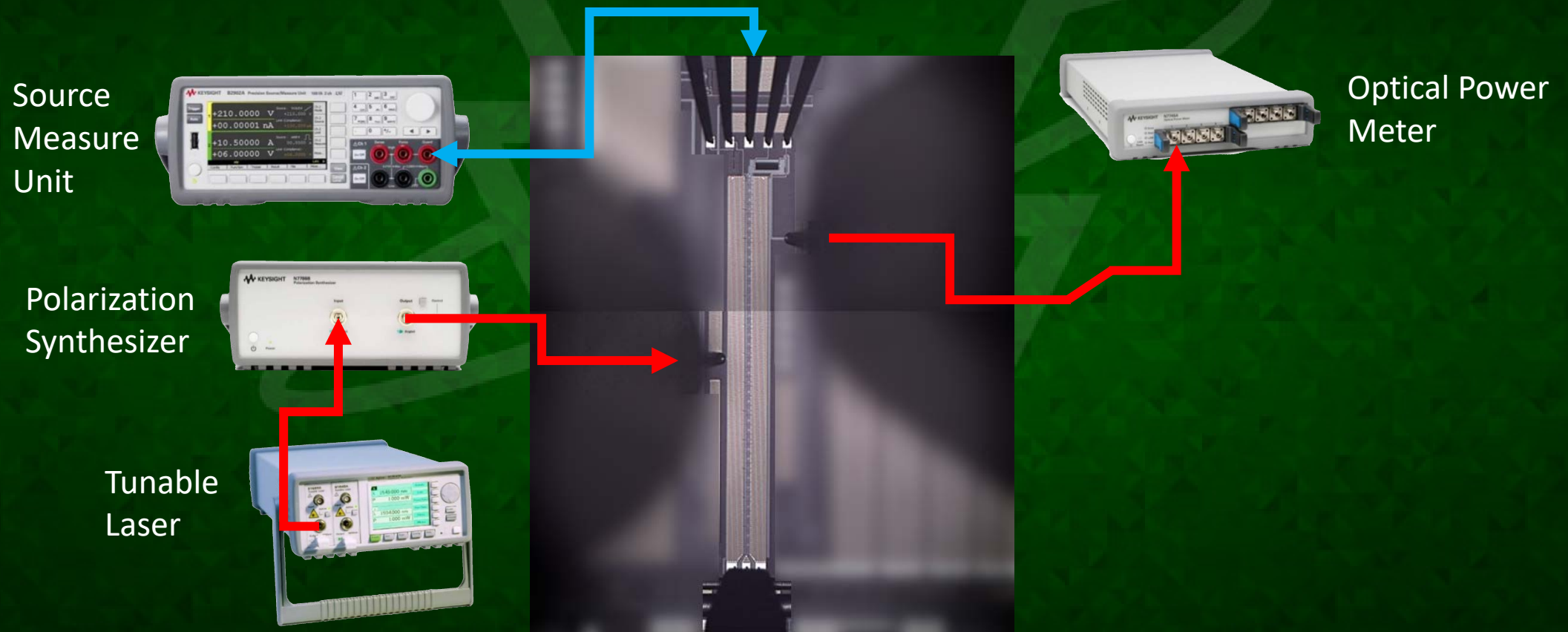
- **Implement Automatic Testing Architecture - Modulator as Example**
  - Peak Search; Optimizing Polarization → Setup optical path



# 3. Achieving Automatic Production Photonics Tests

- **Implement Automatic Testing Architecture - Modulator as Example**

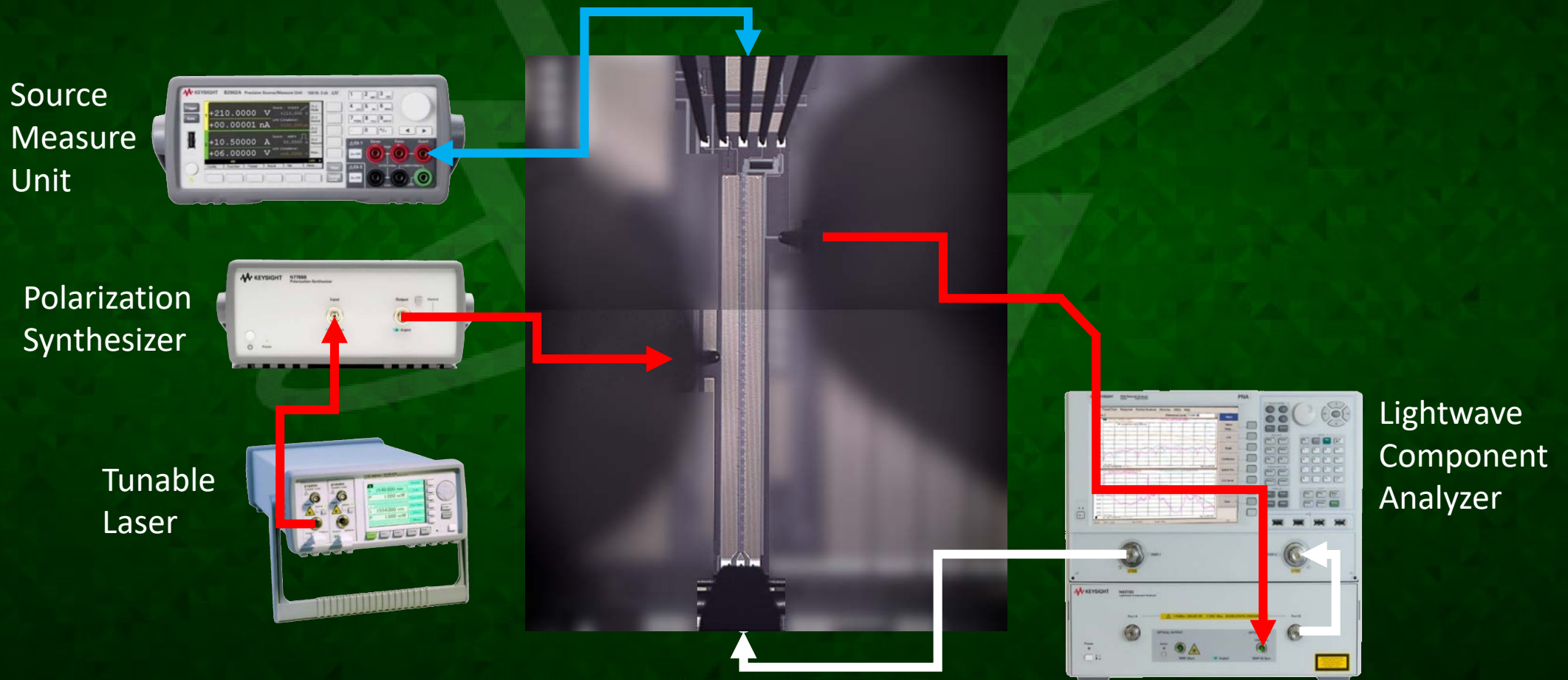
- Bias Tuning to Measure Extinction Ratio (ratio of optical power levels of a digital signal, “1” and “0”)



# 3. Achieving Automatic Production Photonics Tests

- **Implement Automatic Testing Architecture - Modulator as Example**

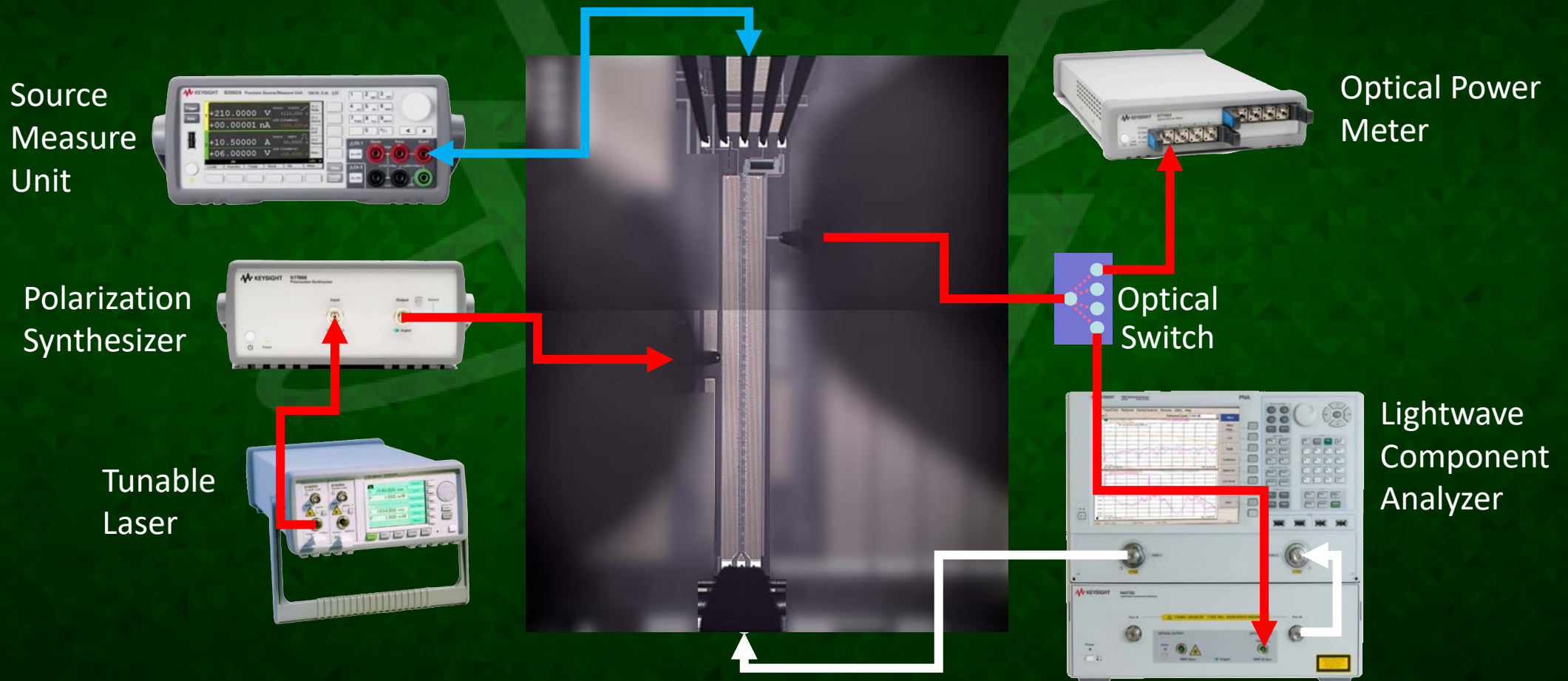
- Connect to LCA for RF Frequency Sweep to Measure Modulator Bandwidth



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# 3. Achieving Automatic Production Photonics Tests

- **Implement Automatic Testing Architecture - Modulator as Example**
  - Instrument Automation implemented with an Optical Switch. (automation vs power budget)



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# 3. Achieving Automatic Production Photonics Tests

The screenshot displays the FORMFACTOR software interface, version 2.0.4, which is used for controlling a photonic testing machine. The interface is divided into several key sections:

- AS Data (Input and Output):** Two 3D surface plots labeled "Input Peak" and "Output Peak" show the topography of the input and output surfaces. Below these are corresponding 2D "GS Data" plots showing "PZT Input Y (um)" vs "PZT Input X (um)" and "PZT Output Y (um)" vs "PZT Output X (um)".
- System Status Indicators:** A section on the bottom left shows the status of various components:
  - Hexapod Moving (Green circle)
  - Nanocube Moving (Green circle)
  - System Initialized (Green circle)
- Power Meter Chart:** A graph titled "Power Meter 0.937" and "Power Feedback" shows the power level over time, with a current reading of 0.937.
- Machine View:** A central camera view shows the physical setup with labels for "DC Probe", "Output Fiber", and "Input Fiber". The status at the bottom of this view is "STEPPING TO DIE #1".
- WaferMap:** A circular grid on the right side displays a "WaferMap" with numerical values for each die location. A small circle highlights a specific die, and a coordinate system (X, Y) is shown at the bottom.

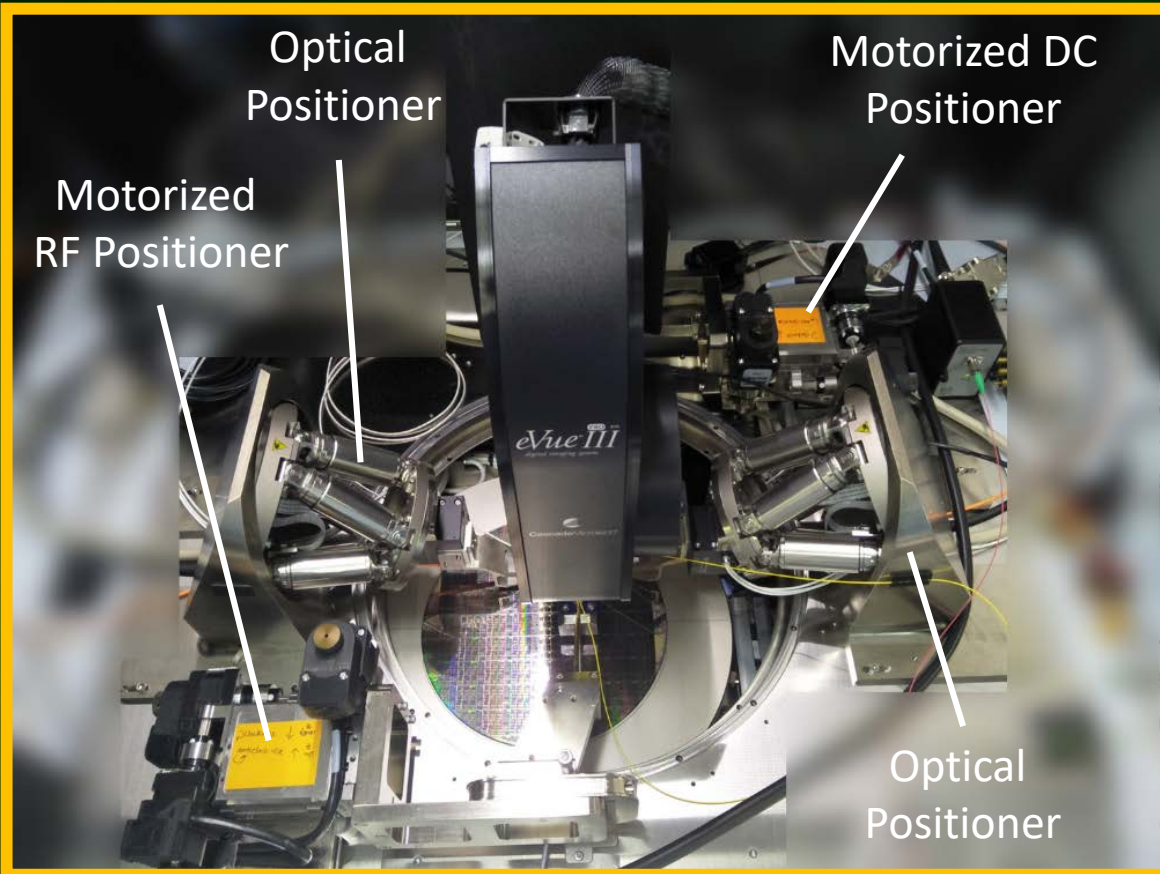
# 3. Achieving Automatic Production Photonics Tests

The screenshot displays the FORMFACTOR software interface, version 2.0.4, used for photonic testing. The interface is divided into several sections:

- Input Peak and Output Peak:** Two 3D surface plots showing the input and output peaks. The input peak is a red, cone-like structure, and the output peak is a similar structure with a slightly different shape.
- In GS Data and Out GS Data:** Two 2D grid plots showing the input and output data. The input plot shows a grid of data points, and the output plot shows a similar grid with a different distribution.
- System Status Indicators:** A section with three indicators: Hexapod Moving (green dot), Nanocube Moving (green dot), and System Initialized (green dot).
- Power Meter Chart:** A line graph titled "Power Feedback" showing power (W) on the y-axis (ranging from -0.3 to 3.8) and time on the x-axis. The power starts at approximately 2.5 W, drops to about 1.5 W, and then fluctuates between 1.0 W and 1.5 W.
- Machine View:** A central view of the machine showing the "DC Probe" and "Output Fiber" connected to the "Input Fiber".
- WaferMap:** A circular grid representing the wafer map. The grid contains numerical values for each cell. A red crosshair is visible on the grid, indicating the current position of the probe.

At the bottom of the machine view, the text "PERFORMING INPUT PEAK SEARCH" is displayed. The software interface also shows a status bar with "Status: Idle" and "Machine is ready to start...".

# 3. Achieving Automatic Production Photonics Tests



- 2 Optical & 2 Motorized DC/RF positioners
- Fully Automatic 300mm Probe System
- Handle diff. layout with remote commands
- Automatic Wafer Loading/Unloading

# Summary

- **Why Huge Demands for Silicon Photonics?**
  - Need for Energy-Efficient Data Centers is driving huge demands for SiPh.
- **Why Wafer-Level Photonics Tests?**
  - Determine Known-Good-Dies & Shorten Product Time to Market.
- **What are the Test Challenges & Possible Solutions?**
  - Must Optimize the Incident Angle for Production Tests.
  - Achieve Good Correlations between Wafer-level & Final Product Tests.
  - Establish Design Rules, Standardize Layout & Implement Automatic Testing Architecture = Fully Automatic Photonics Tests.



# Acknowledgement

- **GLOBALFOUNDRIES Singapore**

- Jun Hao Tan
- Szu Huat Goh
- Jacobus LEO





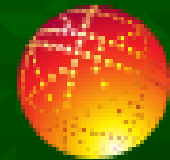
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# Thank You! Questions?



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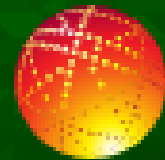
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# Backup Slides



**Dr Choon Beng Sia**  
**[Choonbeng.sia@formfactor.com](mailto:Choonbeng.sia@formfactor.com)**



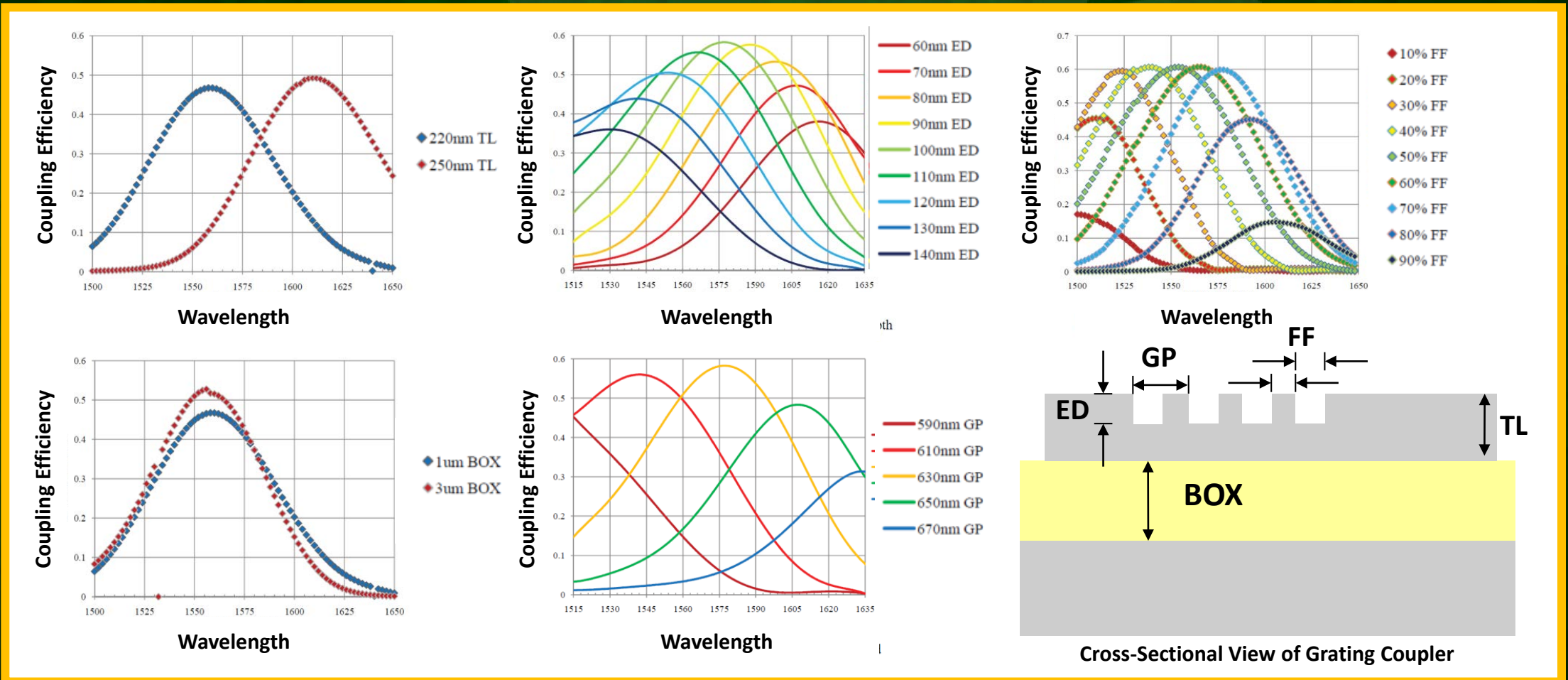
**GLOBALFOUNDRIES**

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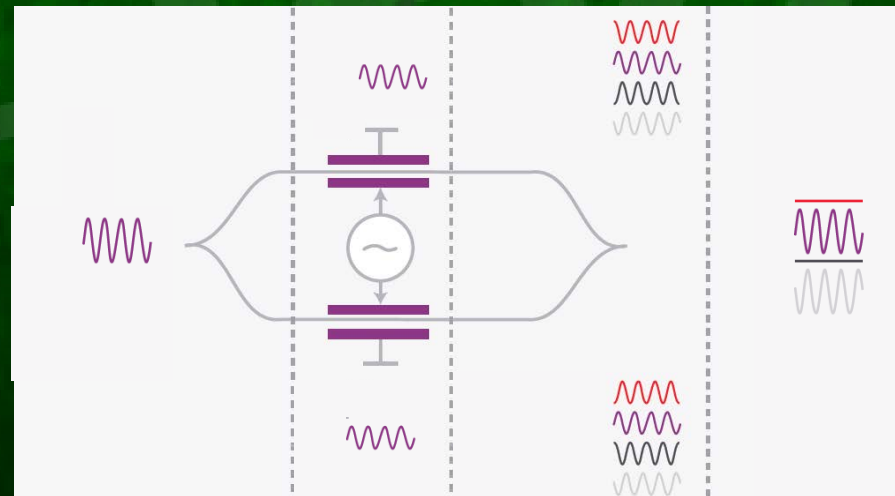
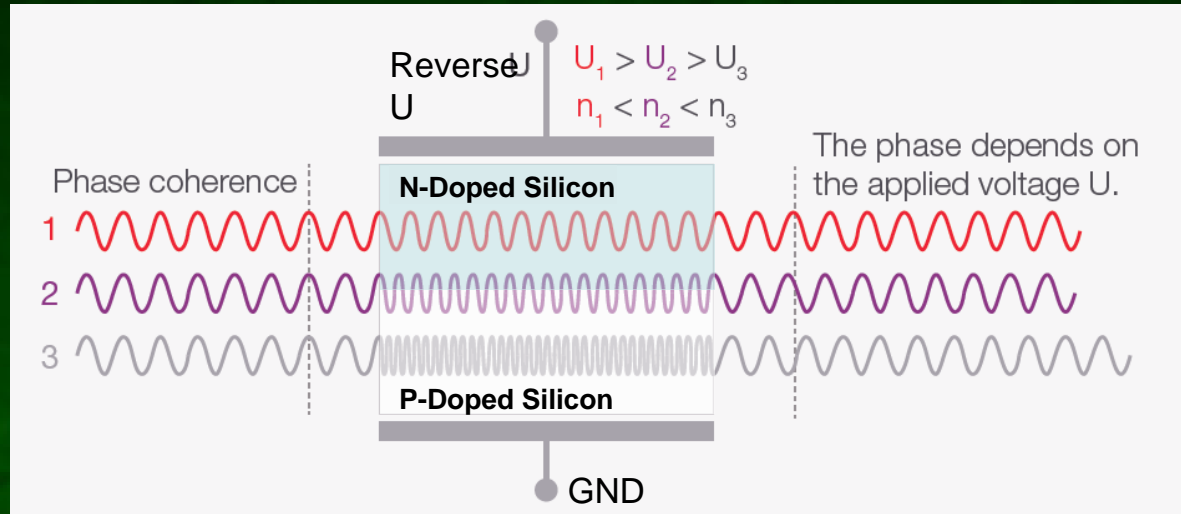
June 2-5, 2019

# Factors affecting Performance of Grating Coupler

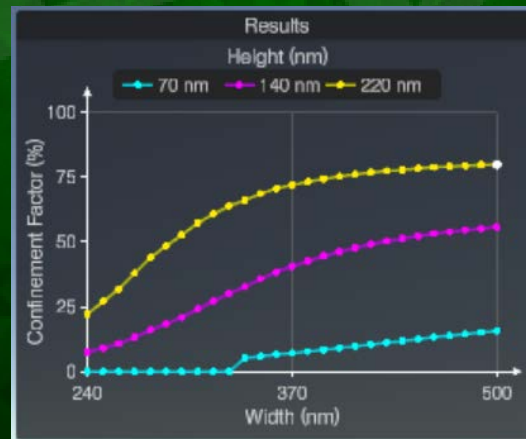
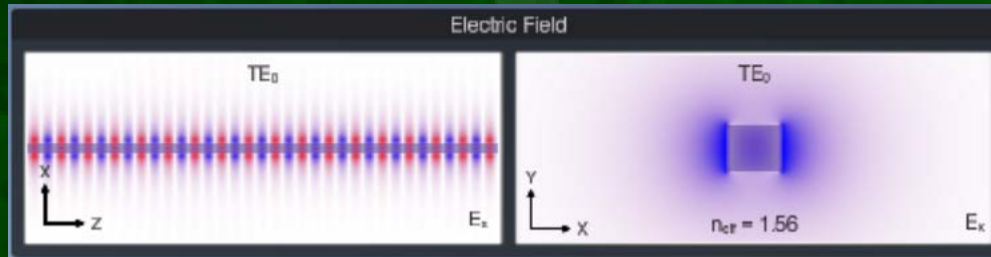
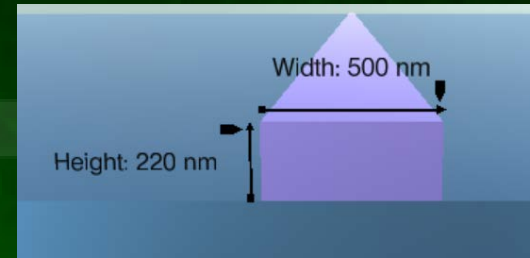
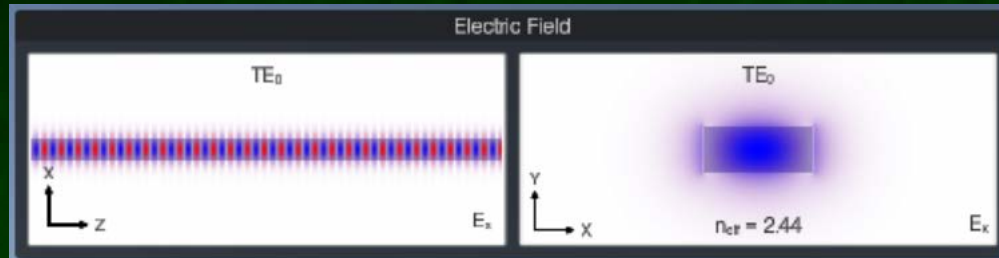
- Top Silicon Thickness (TL), BOX thickness, Etch Depth (ED), Grating Period (GP) and Fill Factor (FF) are known to have impacts on the Coupling Efficiency, Peak Wavelength and Bandwidth.



# Mach-Zehnder Modulator



# Inverse Taper Edge Coupler



# Requirements for Data Center – Energy Efficiency

- **\*Information Technology to consume 21% of Earth's power by 2030.**
  - Data Centers and Wired Access are largest consumers.
- **†3% Total Electricity (in 2016), will double every 4 years.**
  - 24% consumption by 2028?
- **#Governments are now Regulating Data Centers!**

