iFail: Predicting end-of-life for future mobile devices

Dealing with test and measurement in the world of personal electronics

By Timothy McMullen, Director of Product Marketing, Reliability Test Systems, Cascade Microtech, Inc.

Consumer expectations continue to create a relentless challenge for the electronics industry, demanding that each new generation of mobile devices delivers increased performance — more applications, faster speed, and longer battery life — all without sacrificing reliability. To capture their share of the multi-billion dollar mobile electronics market, manufacturers are under great pressure to produce innovative, next-generation products as inexpensively and as quickly as possible.

Pushing the performance and time-to-market envelopes often runs counter to the concept of conservative designs with built-in quality and reliability. To meet performance and cost goals, device manufacturers are forced to pursue creative new technologies such as FinFETs (3D transistors) and 3D IC integration schemes with bumps, pillars, and through-silicon vias (TSVs). But these new design approaches can have serious implications on semiconductor device life and reliability. This is where intrinsic semiconductor reliability testing comes into play, enabling designers to find the sweet spot that optimizes both performance and quality while keeping to a quick production schedule.

What is reliability testing?

Intrinsic reliability testing predicts the long-term viability (Figure 1) of ICs by measuring the wear-out properties of the materials used in manufacturing. Reliability engineers design specialized test structures on the wafer and subject them to a variety of elevated electrical and thermal biases to accelerate their breakdown. Data from these tests are extrapolated to estimate IC life under normal use conditions, and the results of this evaluation inform decisions to qualify fabrication lines and determine safe operating condition rules for IC designers.

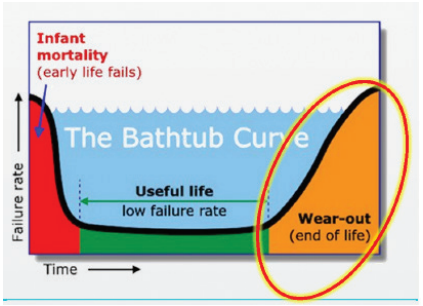

Figure 1. "Bathtub curve" illustrating the realm of intrinsic reliability consideration.

Trends impacting reliability test

For decades, shrinking semiconductor device size was the primary mechanism for achieving performance and cost goals according to "Moore's Law." Years of innovations have driven minimum feature sizes from several microns in the 1980s down to 22 nm in current production, with roadmaps to 5 nm and beyond.

However, simple scaling is reaching practical limitations (Figure 2); to continue miniaturizing, semiconductor manufacturers have introduced exotic materials, processing techniques, and structure types (or "More Moore" technologies) including ultra-low-k intra-level dielectrics (ILDs)

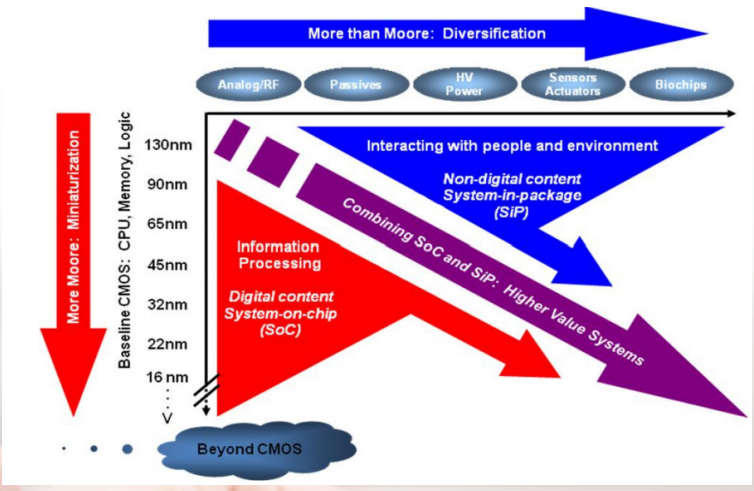

Figure 2. Semiconductor trends affecting reliability.

with various interconnect barrier metals, hafnium-based high-k/metal-gate (HKMG) dielectric gate stacks, and the highly-publicized FinFET transistor structures. IC makers are also introducing game-changing "More than Moore" structural advances such as 3D IC integration schemes that stack multiple dies using solder bumps, copper pillars, and TSVs.

As this drive for innovative solutions continues, and as new technology nodes increasingly diverge from their predecessors, the associated uncertainties must be met with careful reliability testing. These technologies require more from reliability test equipment — new test algorithms, tighter source and measurement accuracy, faster data sampling, and higher test throughput — to bring new technologies to market faster.

Reliability engineers are also shifting away from the traditional package level reliability (PLR) program toward increasing reliance on wafer level reliability (WLR). For PLR, DUTs are sawn from the wafer, individually packaged, and tested in temperature chambers. WLR uses probe stations and thermal chucks to directly test DUTs on intact wafers. PLR remains an essential element of reliability test programs, but the increased interest in the WLR approach is due to faster initial test results, elimination of DUT damage from handling, and lower operating cost, and is further enabled by the capabilities of today's parallel WLR systems.

Key reliability test applications

Intrinsic reliability test applications are often segregated between back-end-of-line (BEOL) and front-end-of-line (FEOL). Some of the most common IC failure modes are electromigration (EM), bias temperature stress (BTS), time-dependent dielectric breakdown (TDDB), and bias temperature instability (BTI).

Electron flow through metal over time causes atoms to dislocate (electromigration), creating voids and extrusions in copper lines and vias, solder bumps, and TSVs. This results in high-resistance connections, localized hot spots, and short-circuits to nearby features causing IC failure. EM tests are most commonly performed as PLR, and modern EM test systems utilize source-measurement unit (SMU) designs with fast measurement sampling, ultra-low-resistance measurement abilities, and ultra-low-current source accuracy.

Ultra-low-k ILDs and barrier layers are targets for bias temperature stress, where an electric field induces barrier layer breach and Cu oxidation, and ultimately short-circuited connections. Time-dependent dielectric breakdown in transistors, including those based on HKMG and FinFET technology, responds to the electric field across the gate oxide with the creation of charge traps that permit current to tunnel through the insulator. This leads to transistor performance shifts and short circuits. BTS and TDDB are often tested with the same equipment, and today's systems employ faster sampling and better measurement accuracy to clearly detect and interpret soft breakdown (SBD) and progressive breakdown (PBD) phenomena. These tests are efficiently performed with both PLR and WLR.

Bias temperature instability is a pressing concern for advanced geometry CMOS transistors, and it results in shifting transistor performance. BTI is believed to occur primarily at the silicon-insulator interface; thin HKMG transistors and especially FinFETs are most likely to experience BTI. BTI includes a transient component that self-heals rapidly after stress is removed from the device, and new test algorithms called "on the fly" or "ultra fast" minimize stress disruptions by using fast equipment and simple measurements to estimate device wear-out rather than directly measure it. Currently, BTI is performed almost exclusively as a WLR test.

Today's IC manufacturers are drawing increasingly finer lines between reliability and performance. It is no longer sufficient to qualify semiconductor lines with a simple pass/fail evaluation. Many IC designers are fine-tuning and optimizing the reliability-versus-performance balance for each individual subsystem within their chips. The delicacy of this balance drives the increased use of WLR and more stringent demands upon reliability test equipment for precision and throughput. Advanced test tools are key to the semiconductor industry's campaign to bring more sophisticated, reliable mobile products to market faster. ECN