Quantum Computing IC Die Level Test Solution at mK Temperature Environment

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Overview

- Introduction: Global Quantum-Related Market Size & Ramp-up Applications
- Quantum IC Trend & Die Level Testing Challenge
- Kobe University Quantum IC Test Case
- FormFactor PQ500 Probe Socket – A Quantum IC Die Level Testing Solution
    - Probe to PAD Alignment (Room Temp to mK Temp)
    - DC Resistance Characterization between Room Temp and 4K Temp
    - Electrical Simulation with Cryogenic Temperature Material property
    - Data from Kobe Universty for PQ500 Product Validation
- Future Development Directions and Acknowledgements

Raising Quantum Computing Era

Rapid Growth Market with 4 Key Applications

By 2030 Quantum Computing Market Size Estimated to be $125B

36% CAGR 10 Years Projection

TENTATIVE QUANTUM COMPUTING APPLICATIONS – ROADMAP

	2023–2030	2030–2040	2040–
Machin Learning		Small-scale fraud detection	Vehicle routing; Robotic vehicles; Large-scale fraud detection; Weather forecast
Optimization	Financial risk mitigation; Supply chain; Logistics	Price prediction; Investment portfolio; Risk management	Vehicle routing
Simulation	Small-scale protein folding and molecular docking	New materials; Small molecules	Large molecules; Electronics; Genomics; Large drugs
Communication	NIST Standard	Quantum Modems	Quantum Internet

Risk Management

Cybersecurity

Material & Fluid Dynamic

Drug Discovery

PRECEDENCE RESEARCH

QUANTUM COMPUTING MARKET SIZE, 2021 TO 2030 (USD BILLION)

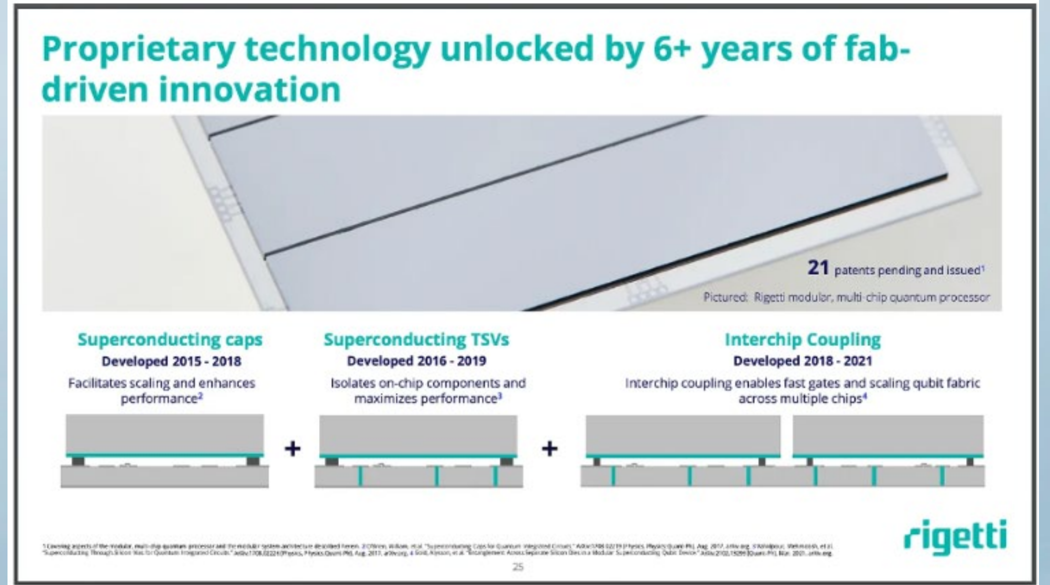
36% CAGR 10 Year Projection

Year	Market size (USD billion)
2021	$ 7.4
2022	$ 10.13
2023	$ 13.87
2024	$ 18.98
2025	$ 25.98
2026	$ 35.57
2027	$ 48.69
2028	$ 66.65
2029	$ 91.23
2030	$ 125

Source: www.precedenceresearch.com

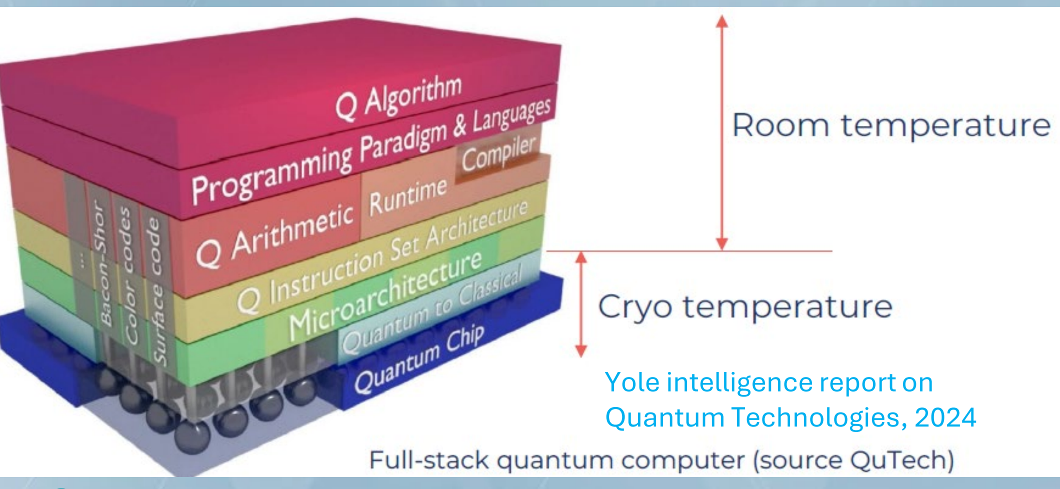
Credit: Yole intelligence report on Quantum Technologies, 2024

Scale Quantum Computing Power with Advanced Packaging Technology – Demanding More Test?



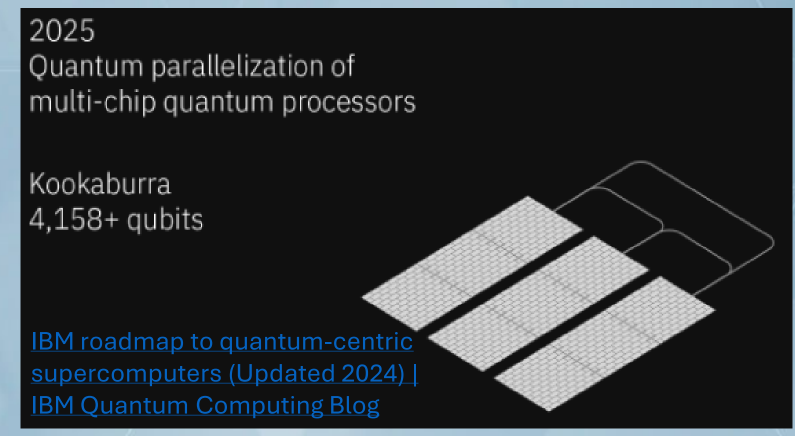
Quantum Computing + Advanced Packaging

- Increasing Quantum Computing Power
  - Couple application layers with quantum computing
    - Superconducting, Silicon Photonics etc…
  - Grow # of qubits by packaging multiple Quantum ICs
    - X3 expanding number of qubit
- Testing Quantum Computing ICs at the die level
  - Low yield, high packaging costs demand more test
  - Known good quantum ICs before packaging with others
  - Lower cost of test, real performance data, faster lead times

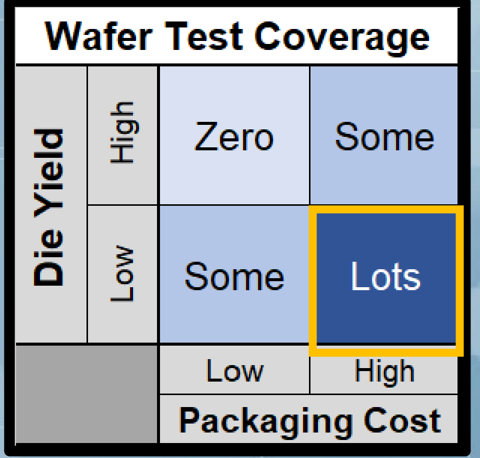


Yole intelligence report on Quantum Technologies, 2024

Full-stack quantum computer (source QuTech)



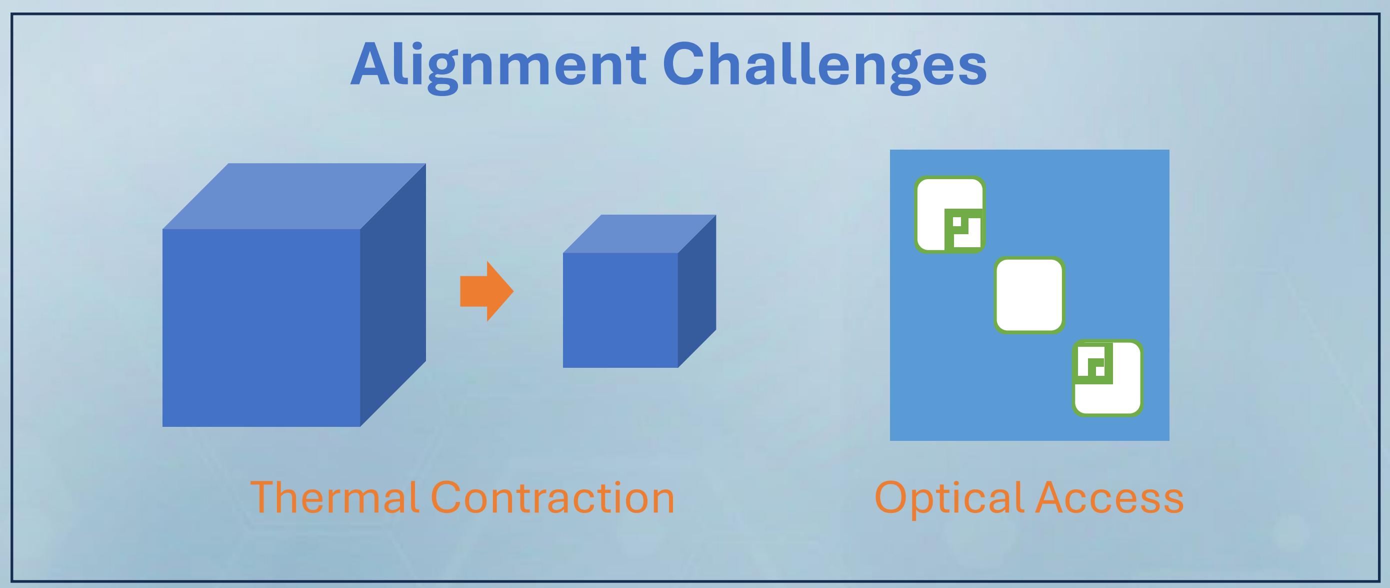
IBM roadmap to quantum-centric supercomputers (Updated 2024) | IBM Quantum Computing Blog

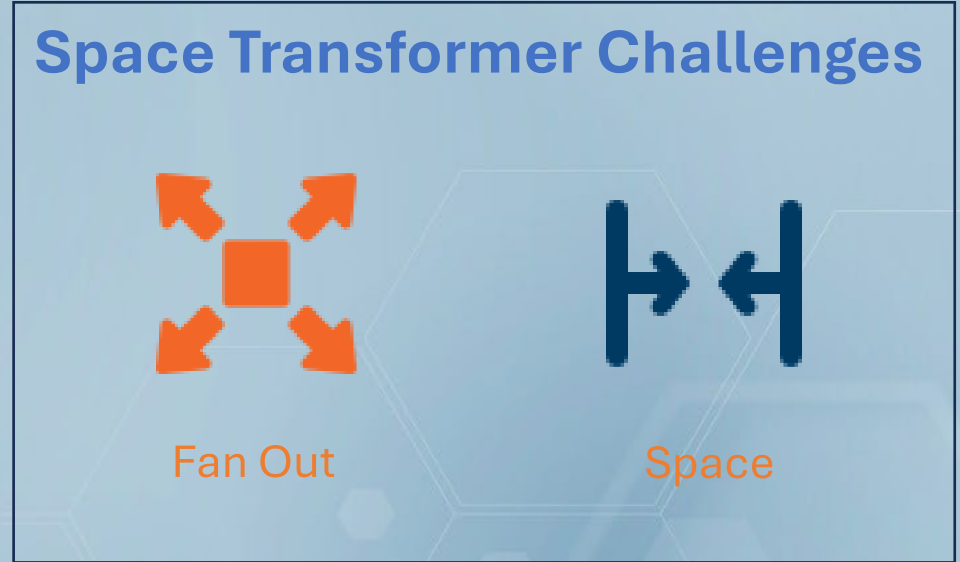


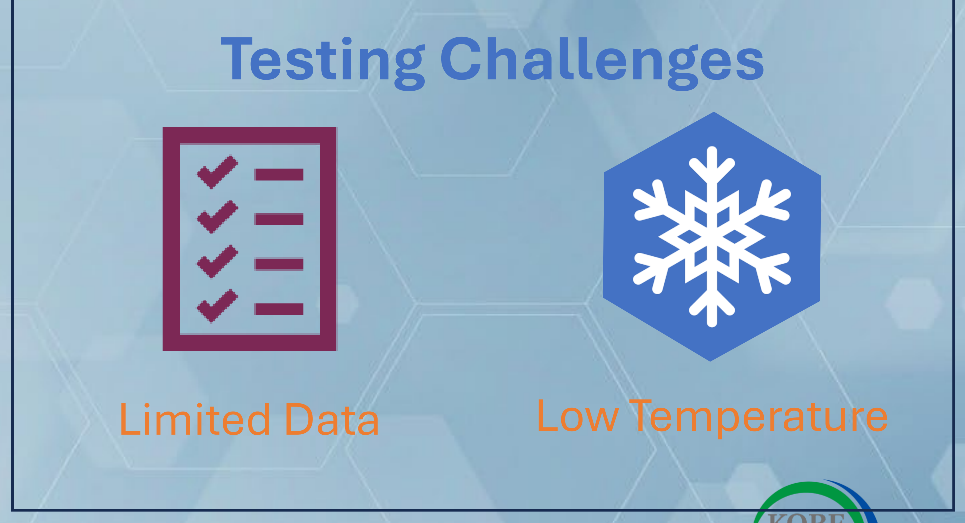
Wafer Test Coverage

Die Yield			
	High	Zero	Some
	Low	Some	Lots
		Low	High
		Packaging Cost	

Quantum IC Die Level Probing Challenges

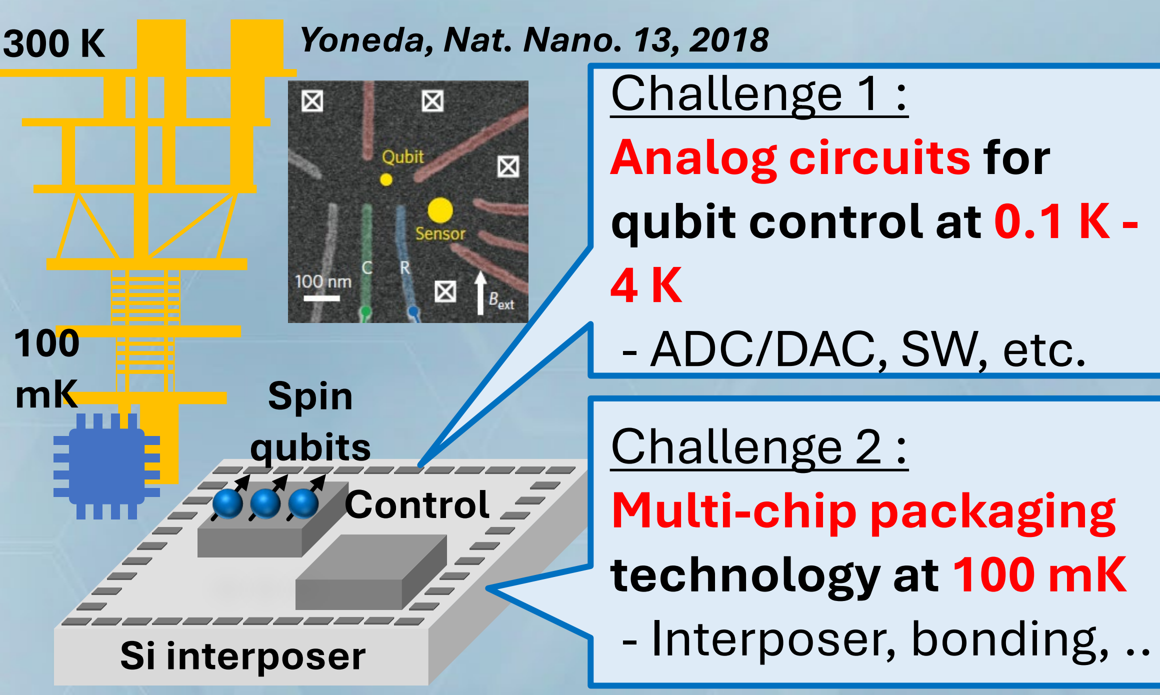






Kobe Case Application

- **Silicon quantum computer**
  - **Scalable : compatible with CMOS**
  - **Long coherence time**
  - **Thermal stability : >100 mK**



Challenge 1 :
Analog circuits for qubit control at 0.1 K - 4 K
- ADC/DAC, SW, etc.

Challenge 2 :
Multi-chip packaging technology at 100 mK
- Interposer, bonding, ..

- **Test requirements**
  - **Deep cryogenic temperature below 1 K**
  - **Short cooling time**
  - **Numerous DC**
  - **Up to 20 GHz RF**

FormFactor ADR Cryostat

- 20 mK lowest
- 15h rapid cool

PQ 500 Socket

- $10mm^2$ chip
- 184-PAD
- 100-DC
- 17-RF

PQ500 Cryogenic Probe Socket

Solution for Quantum IC Die Level Testing

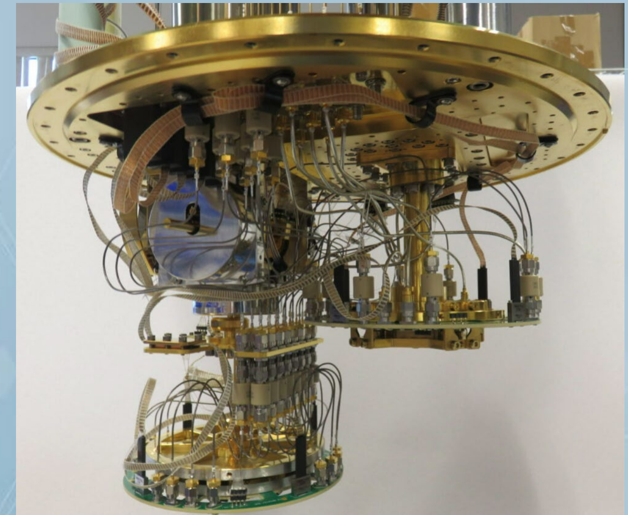
Overview of PQ500 Product and Benefits of Die Level Testing

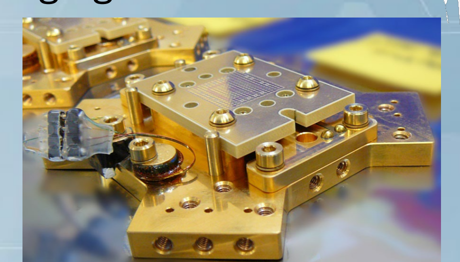
A first-of-its-kind, cryostat-agnostic, high-density RF and DC socket interface

- Customized design to fit on FormFactor cryostat/DR or customer existing cryostat/DR
- Offer probing solution under mK cryogenic temperature environment
- Socket design option for magnetic field shielding
- World class Vertical MEMS Probe supports 150 um pitch pad/bump probing
- **Active alignment** feature ensure the solid contact to the PAD
- Easy operation – undock the socket while all RF connection remain the same
- Product validated under cryogenic temperature before shipment

Benefits of using PQ500 test at die level

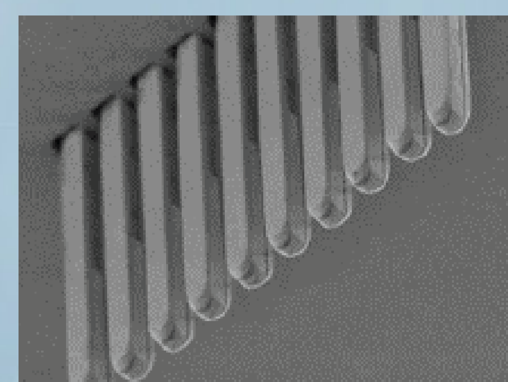
- Test and validate performance directly on silicon without post-dicing packaging
- Dramatically reduces time to data and shortens development cycles
- Enables high scalability for high volume manufacturing
- Offers flexibility in chip design with full grid probing

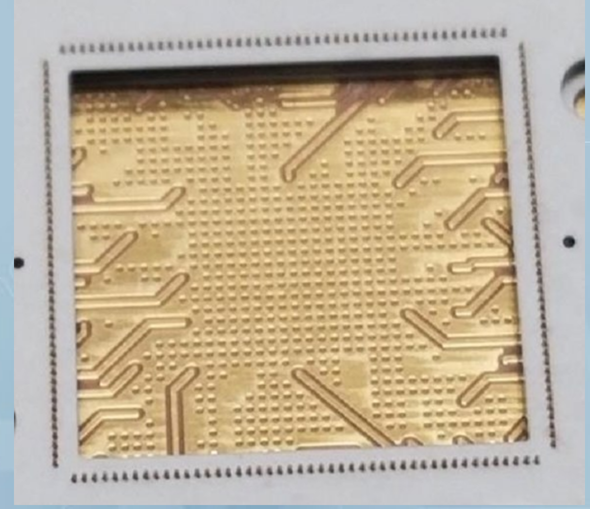




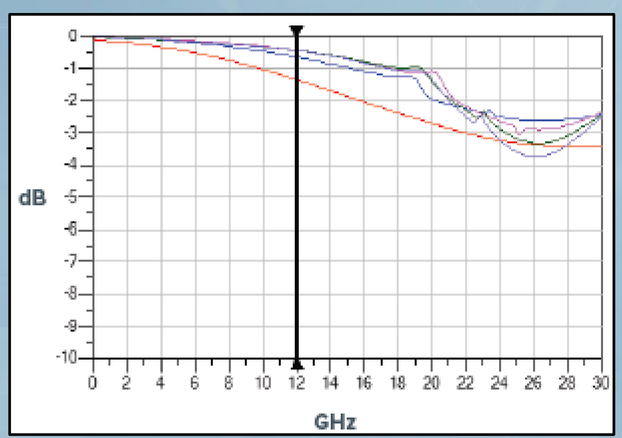
Cryogenic Vertical MEMS Probe GC150

Probe model	GC150 Vertical MEMS Probe
Probe metallurgy option	Non-ferromagnetic
Probe tip dimension	25 µm x 30 µm
Min. pad/bump pitch - grid array	150 µm x 150 µm
Probe head deployment temperature	mK to 400 K
Signal type	DC and/or RF (<20 GHz)
Max. device size	50 mm x 50 mm
Compatible device pad material	Al, Au, Cu
Probe tip planarity	25-35 µm
Probe-to-pad/bump alignment precision	±12.5 µm
Recommended overdrive	75-100 µm
Probe force within recommended overdrive	3 gforce
ISMI current carry capability	1.4 A

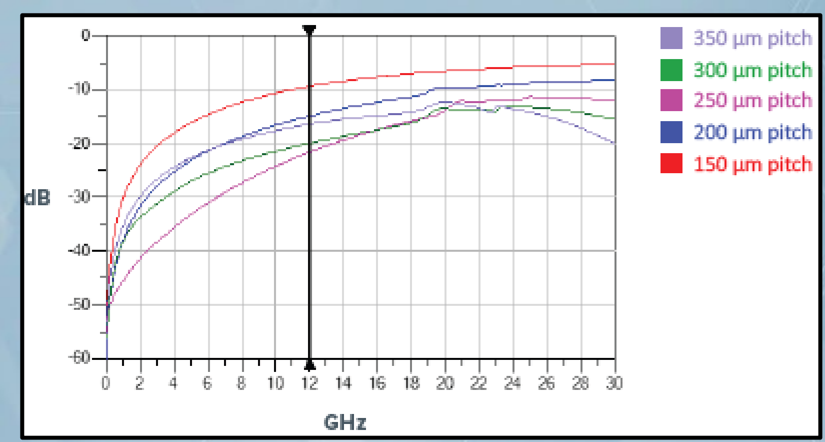




GC150 Insertion Loss GSG Config



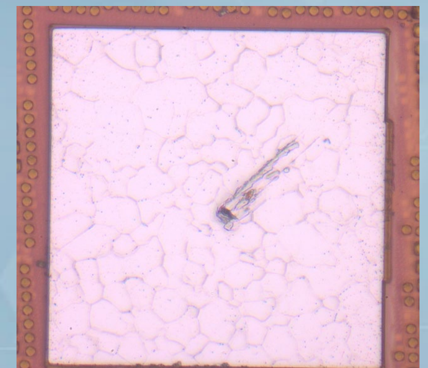
GC150 Return Loss GSG Config



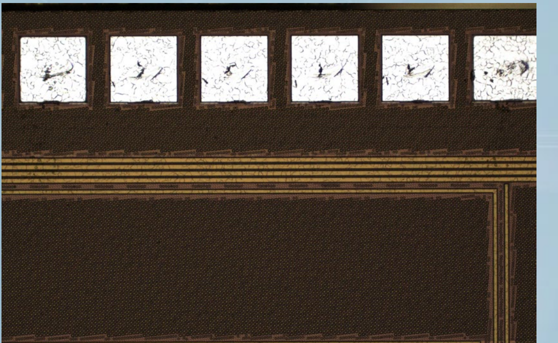
Align Probe Tip To PAD

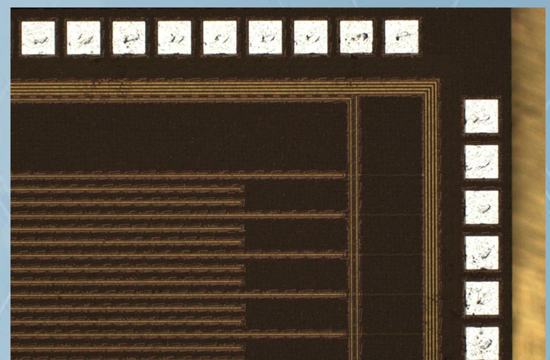
- **Custom finger design hold device sit on heat spreader surface**
  - Multiple adjustment features allow the heat spreader to move in the XY plane and rotate with micrometer-level accuracy
  - Aligning device pad to the scrub mark on grass
- **Scrub Mark from Room Temp to mK Temp**
  - Pad size 150 um x 150 um
  - Probe Tip size 30 um x 25 um
  - Initial alignment done at room temp
  - Probe tip scrub toward to center as temperature go down to 4K

Scrub Mark after Alignment
RT → 4K → RT



Scrub Mark after Testing
RT → mK → RT



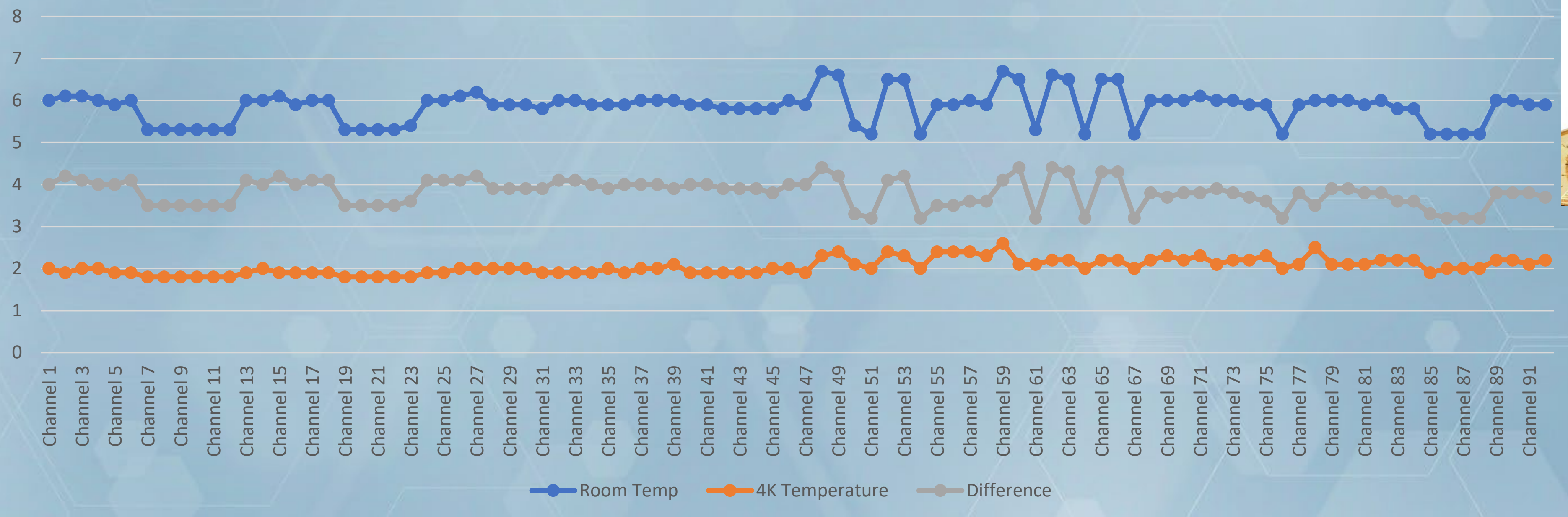


Contact Resistance Characterization

Room Temp vs. Cryogenic Temp

- **Data Collected from Customer using PQ500 Test Socket with FormFactor IQ2000 Cryogenic Prober**
- **Device with 92 Channels: Resistance average drops ~3.8ohm, conductivity improves 65%**
  - At room temp: measured resistance average ~5.8ohm
  - At 4K temp: measured resistance average ~2.0ohm
  - Resistance reduce at 4K temperature average ~3.8ohm

Contact Resistance Measurement Room Temp vs. 4K Temp



PQ500 Electrical Performance Simulation

Product Feasibility Analysis

m8 m7

m7
freq=20.00GHz
IL_room=-7.728dB
IL_Cryogenic=-6.223dB

freq, GHz

m6 m5

m5
freq=20.00GHz
RL_room=-5.133dB
RL_Cryogenic=-3.139dB

freq, GHz

Final Design

m1

m7
freq=20.00GHz
IL_room=-4.809dB
IL_Cryogenic=-2.808db

freq, GHz

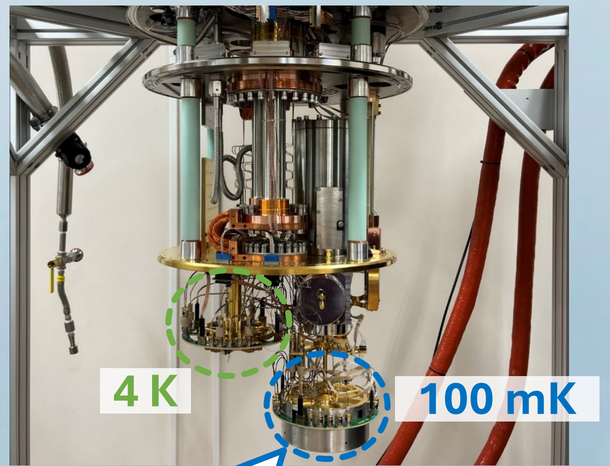
m2

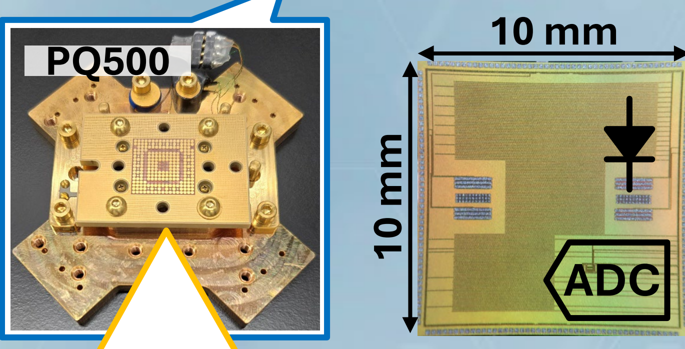
m2
freq=20.00GHz
RL_room=-9.405dB
RL_Cryogenic=-7.465dB

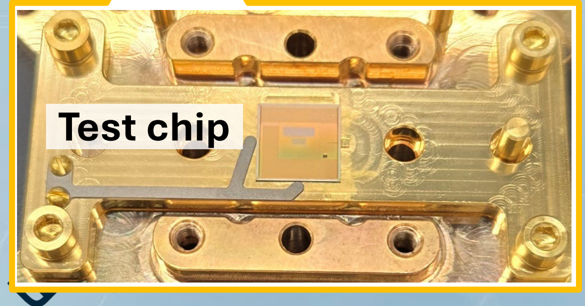
freq, GHz

PQ500 Product Validation at Kobe

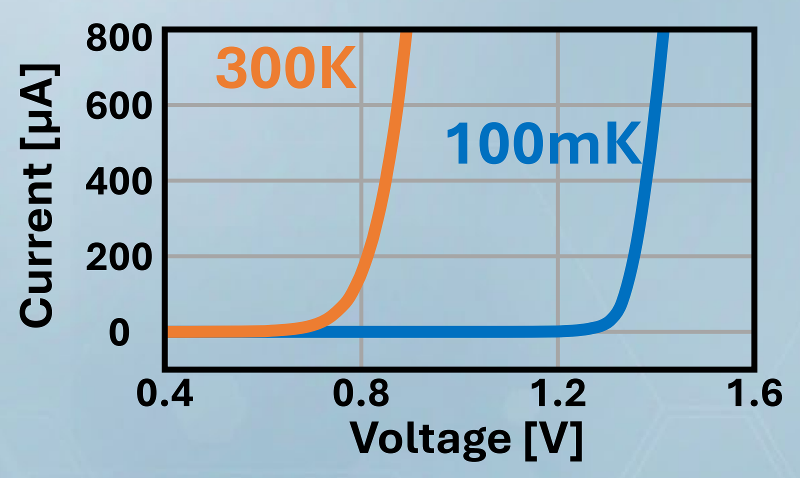
- Test setup





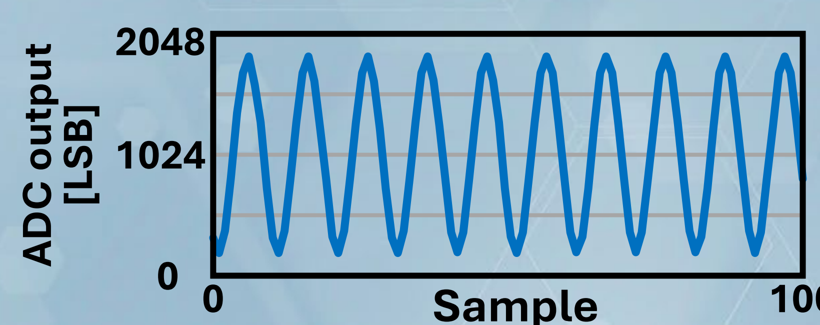


- Cryo Analog Circuits
  - Diode characterization



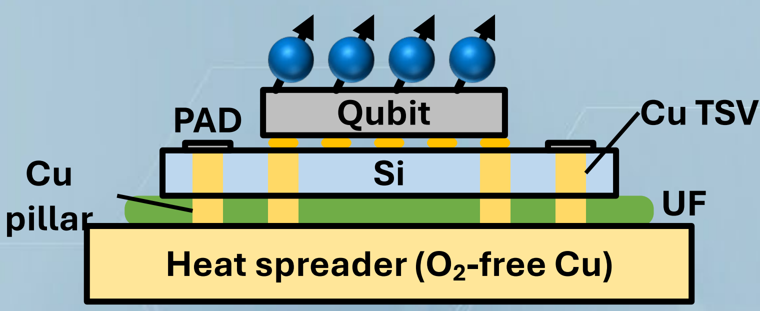
- Cryo-ADC measurement
  – Successful ADC operation at 4K

Takahashi, SiQEW 2024

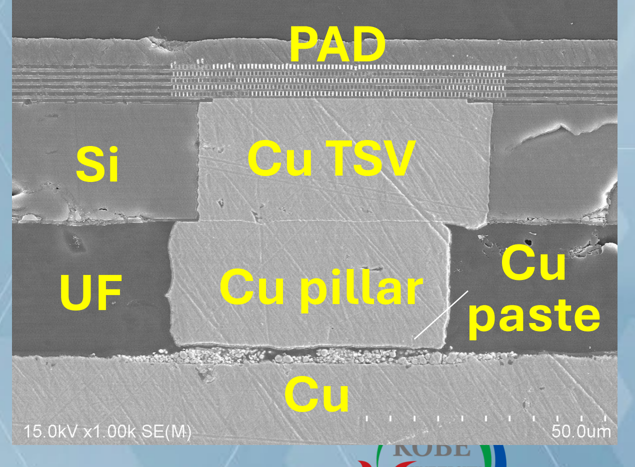


- Cryo multi-chip packaging

Taguchi, ECTC 2024



- Cross section view after thermal cycle
  – Successful Cu-Cu bond via TSVs



Summary & Future Development Direction

- Quantum computing is a rapidly growing industry
- Demand for testing is rising due to challenging requirements
- Probing at the die level shortens time to data and provides real data on silicon performance
- The FormFactor PQ500 has demonstrated a quantum IC die-level test solution in a mK temperature environment with a 20 GHz test speed
- Ongoing efforts aim to improve probe tip-to-pad alignment robustness while continuing R&D on smaller pad/bump pitches and higher-speed testing

Thank You for Your Support !

Acknowledge to the personnel contribute to this project

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