FormFactor™

SWTest Asia Tech Talk

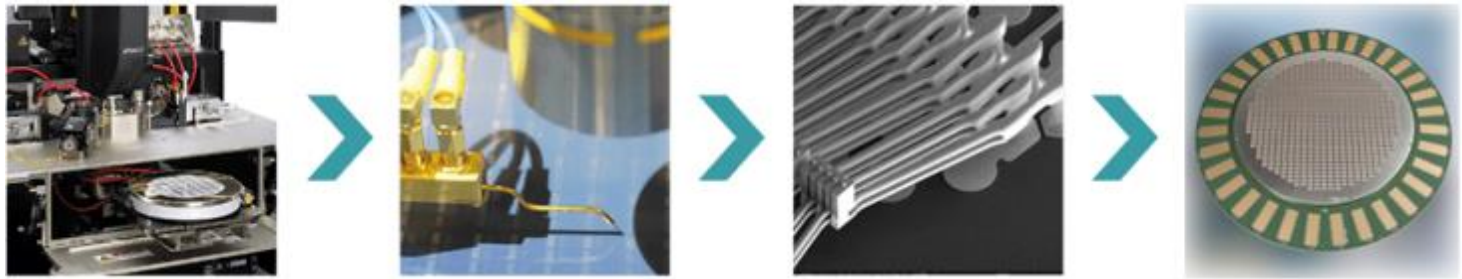
Productivity Innovations for Wafer Test

Amy Leong (CMO, Formfactor)

FormFactor: Leading in Electrical Test and Measurement

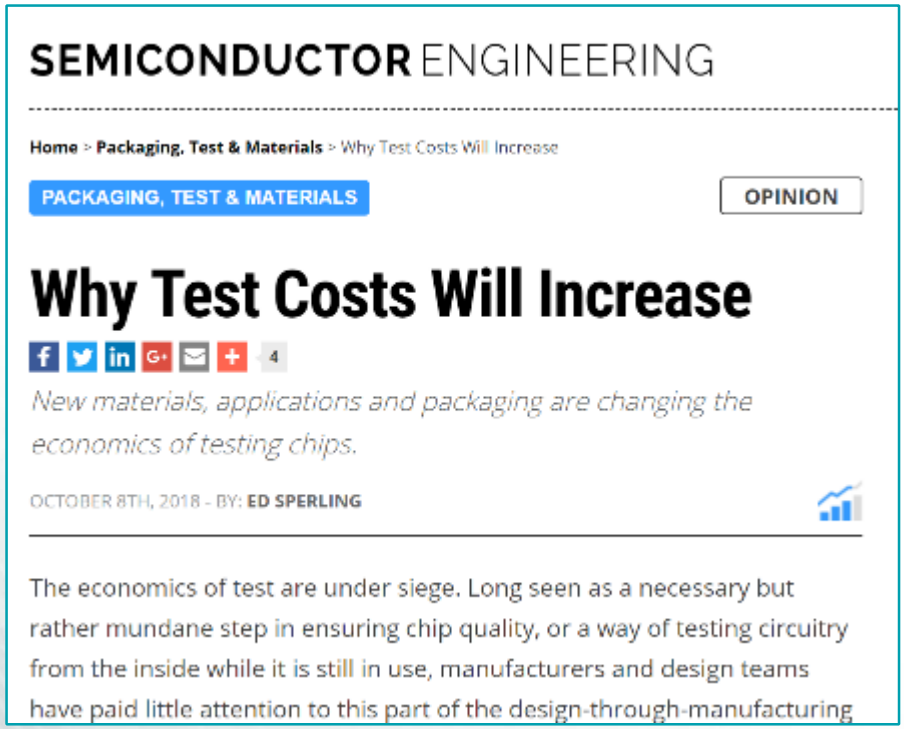
- #1 supplier in advanced probe cards and engineering probe systems with annual 2017 sales of $548M
  - Shipped >45 million MEMS probes in last 12 months
  - >10,000 probe systems installed worldwide
- Named in VLSI Research's THE BEST Suppliers customer survey for the 5th consecutive year
- Leveraging scale and global presence to efficiently drive the roadmap ahead
  - ~1600 employees, about 1/3 directly support customers
  - Largest R&D spend in served markets of ~15% of revenue, directed by key-customer collaborations

Test Insight from Lab to Fab



Engineering/Development | First Silicon | Ramp | Production

Challenges Ahead For Our Test Community
How to Achieve Complex Test Requirement At a Reasonable Cost



SEMICONDUCTOR ENGINEERING

Home > Packaging, Test & Materials > Why Test Costs Will Increase

PACKAGING, TEST & MATERIALS

OPINION

Why Test Costs Will Increase

New materials, applications and packaging are changing the economics of testing chips.

OCTOBER 8TH, 2018 - BY: ED SPERLING

The economics of test are under siege. Long seen as a necessary but rather mundane step in ensuring chip quality, or a way of testing circuitry from the inside while it is still in use, manufacturers and design teams have paid little attention to this part of the design-through-manufacturing

A few examples of complex test requirement…

- Automotive
  - -55C to 175C
  - High power test (1s~10s of kV, 100s of A) + thin wafer
  - Optical + Electrical Test for lidar
  - “Zero Defect” expectation
- 5G
  - Parallel RF from sub-6GHz to 40+GHz
  - RF Calibration to ensure signal integrity
- Wearables
  - Tiny die and bumps sizes (i.e. MicroLED, <10um)
- Advanced packaging
  - KGD wafer test for Heterogenous Integration
- Artificial Intelligence (AI) chips
  - Current Carrying Capability >> 1A per probe

Example 1: Emerging Silicon Photonic Wafer Test
Collaboration is Key to Reduce Measurement Time from Months to Days

Nasdaq

Our Businesses ▼ Quotes ▼

FormFactor Collaborates with Keysight Technologies and GLOBALFOUNDRIES to Deliver Silicon Photonics Test and Measurement Solution

Vote up AAA

Proven, integrated solution features FormFactor's Cascade CM300xi Probe System and Keysight's Photonics Application Suite

LIVERMORE, Calif., June 19, 2018 (GLOBE NEWSWIRE) -- FormFactor, Inc. (NASDAQ:FORM), a leading electrical test and measurement supplier to the semiconductor industry, announced today the company has deployed an integrated CM300xi probing solution for wafer-level testing of silicon photonics (SiPh) devices. Teams from GLOBALFOUNDRIES, FormFactor and Keysight worked together to ensure the system is flexible to meet engineering needs and to deliver high throughput in volume production.

See reactions to FORM
View Print Version
More from GlobeNewswire

- FormFactor to Participate in the 10th Annual CEO Investor Summit 2018
- FormFactor Collaborates with Keysight Technologies and GLOBALFOUNDRIES to Deliver Silicon Photonics Test and Measurement Solution
- FormFactor Announces Breakthrough Improvements in Productivity for RF Probe Systems

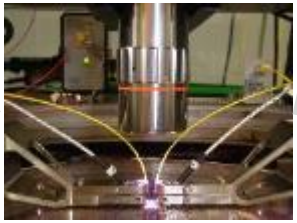
Referenced Stocks

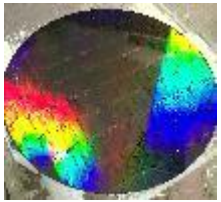
- FORM 75% Rate It

FormFactor™

KEYSIGHT TECHNOLOGIES

Integrated Optical Probing Solution



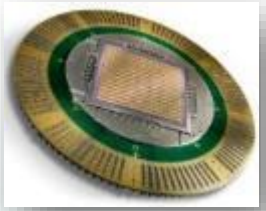


Auto SiPh Solution enables customers to be **measuring** photonics devices **in days** instead of weeks to months

GLOBALFOUNDRIES

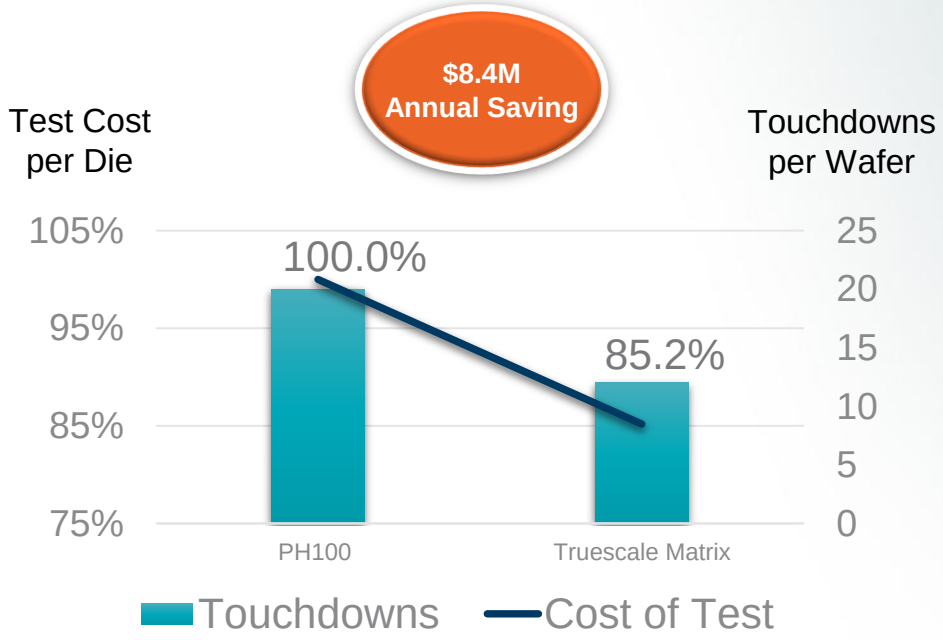
Example 2: Automotive Microcontroller Production Probing
300mm Full-Wafer MEMS Probe Card to Reduce Test Cost

- **Challenge:** High test cost due to long test time and multi-temp
- **Solution:**
  - Increase test parallelism to reduce test cell investment
  - Same probe card for hot (160C) and cold (-40C) testing
- **Results**: $8.4M Annual Test Cost Saving



64-DUT Parallel Test
PH100 Probe Card
100mm Testing Area

95-DUT Parallel Test
TrueScale Matrix Probe Card
300mm Test Area



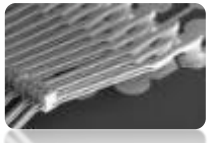
Example 3: Advanced Packaging 2.5D/3D Testing

FFI Offers a Suite of Products to Achieve Optimal Yield And Test Cost From Lab to Fab

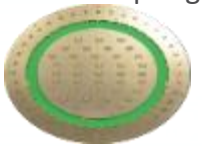
Pre-Singulation Al pad **PRODUCTION** test

Post-Singulation uBump **R&D** test

Matrix Probe Card



T11 MicroSpring



2.2GHz KGD

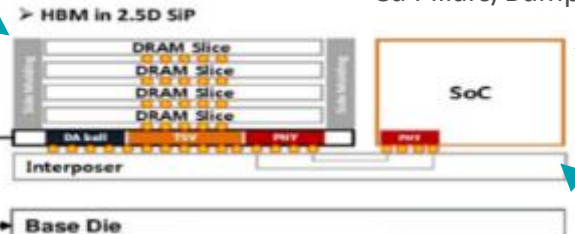
Direct Access uBump Probing

DRAM/HBM

Al/Cu Pads

SoC

Grid-array Sacrificial Pads
Cu Pillars/Bumps

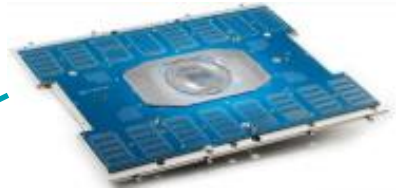


Base Die

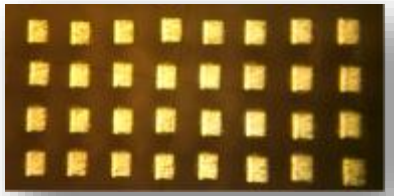
Direct Access Al/Cu Pads
or uBumps

Si Interposer

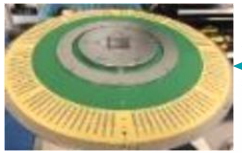
Grid-array uBumps



Apollo Probe Card



Vertical MEMS Probe Tips



NEW

Altius Probe Card for Si Interposer

Example 3: Advanced Packaging 2.5D/3D Testing

FFI Offers a Suite of Products to Achieve Optimal Yield and Test Cost From Lab to Fab

Published work with imec

imec

Dual-loader Configuration

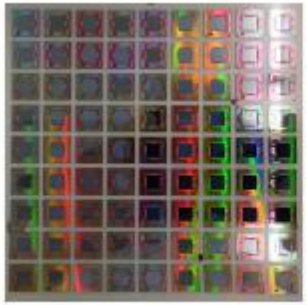
- Two probers: left/right
- Shared MHU auto-loader

Substrate Loading

- Via auto-loader
  - Ø300 mm wafers
- Via front-side load port
  - Wafers up to Ø300 mm
  - Tape frames for wafers up to Ø300 mm

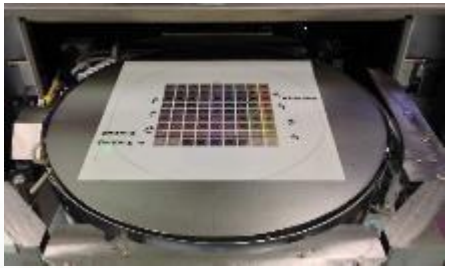
Temperature Rating

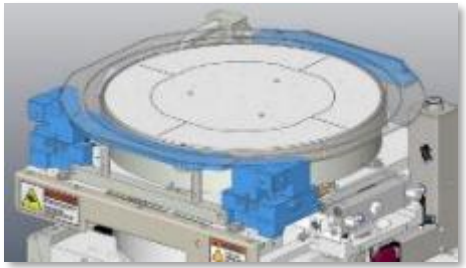
- -65C to 300C



(a) Top-view photo.

(b) Wafer map.





FormFactor 2017-2018 SWTest Asia + San Diego Publications

- Overcoming Challenges for 5G Production Test, by FFI
- 5G: The Next Disruptive Technology in Production Test, by FFI and Intel
- Enabling High Parallelism in Production RF Test, by FFI
- Evaluation of RF Calibration Substrate Lifetime and Accuracy for mW test, by FFI

- MicoLED Wafer Test, by FFI

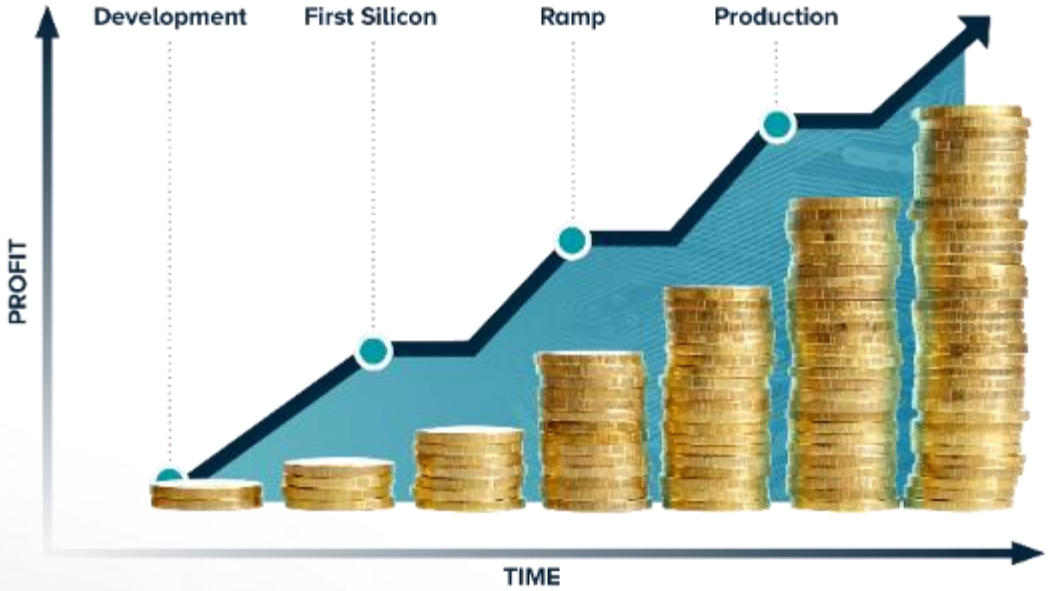
- Break the Myth of Wafer Probing on Cu for FOWLP, by FFI and Samsung
- Verification of Singulated HBM2 Stack with a KGS Test Cell, by FFI and Advantest

- Hybrid MEMS Probe Design to Max Test Performance, by FFI and Qualcomm

Together, We Can…
Accelerate IC Innovation to Profitability From Lab To Fab

Maximum Performance @ Reasonable Cost

Highest measurement fidelity and fastest time-to-results



Required Performance @ Lowest Cost

Meet technical requirements, but minimize risk and cost of test