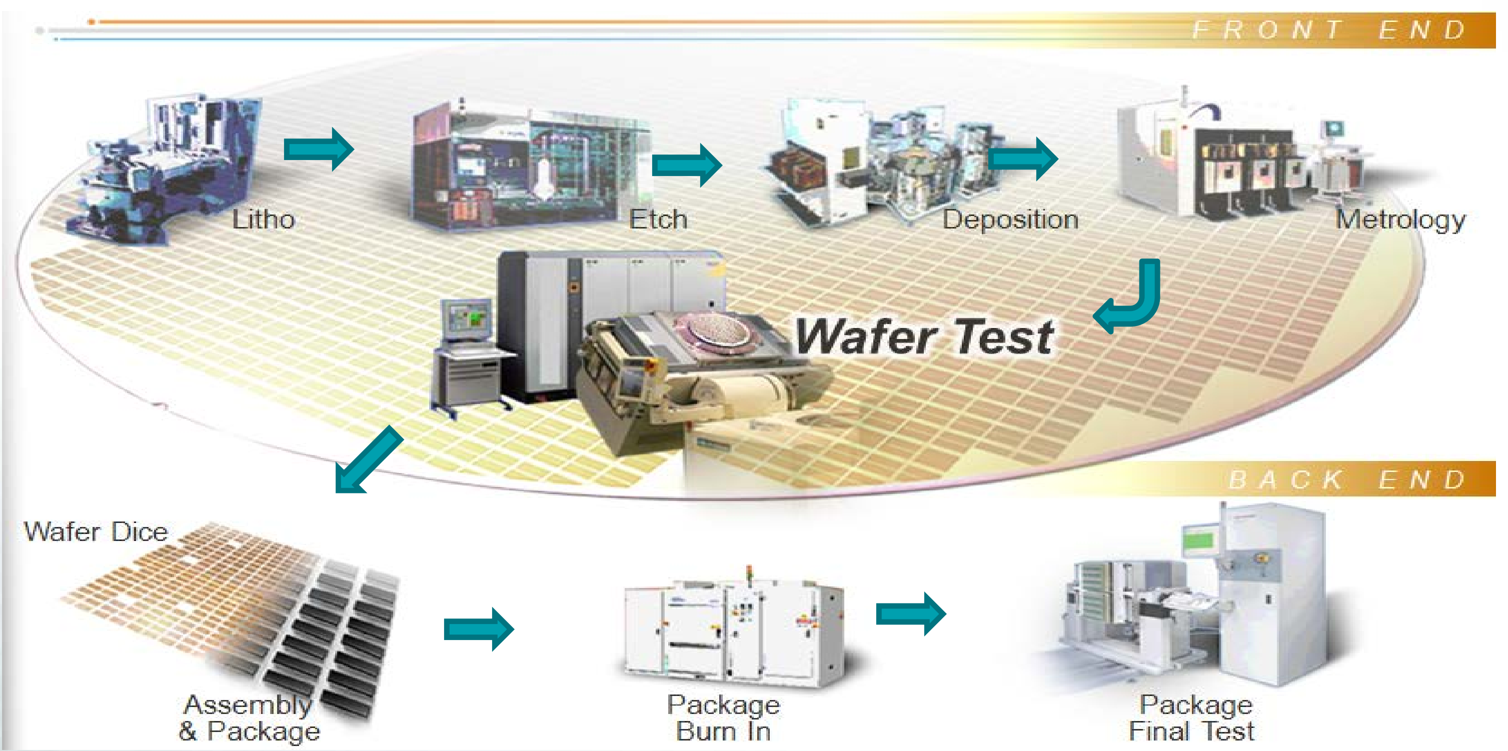
MEMS Probe Technology for Fine-pitch CuPillar Bump Wafer Sort Test

CONFIDENTIAL

Agenda

- Introduction
- Market overview
  - SoC chip packaging trend & driving force of CuPillar packaging
  - Test challenges on fine pitch CuPillar HVM probing
- FormFactor Apollo MEMS MF Probe Product Introduction
  - MEMS Probe Alignment Control
  - Vertical and Lateral Probe Force Impact Probe Mark
  - 2x Current Protection on MEMS Probe
  - MEMS Probe Life-time Projection
  - Automated machine probe insertion
  - Case studies:
    - probe card uptime, probe lifetime data, yield comparison
- Conclusion
  - Formfactor Product portfolio and 2017 Market Share
  - conclusion

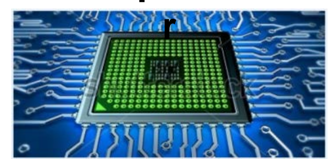
Introduction:
Where does Probe Card Needed in IC FAB Flow



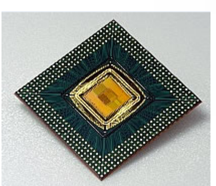
Introduction:
IC Packaging Technology – What're We Probing on

Memory & IOT Chips

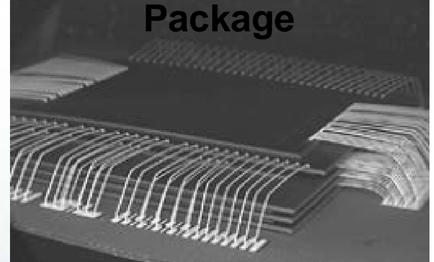
Large Pitch Microprocessor



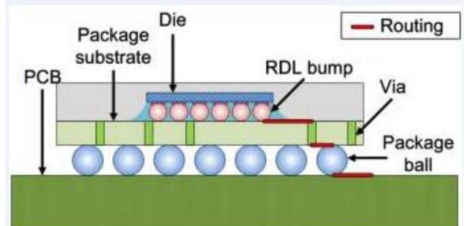
Fine Pitch CPU & Mobile Processor



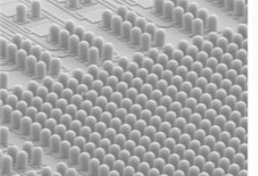
Wire-Bound Package



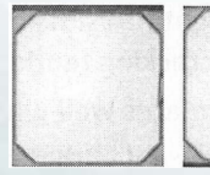
BGA Flip Chip Package



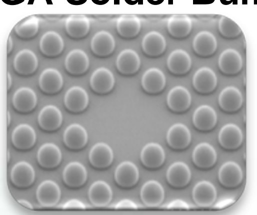
CuPillar Flip Chip Package



Al/Cu PAD



BGA Solder Bump

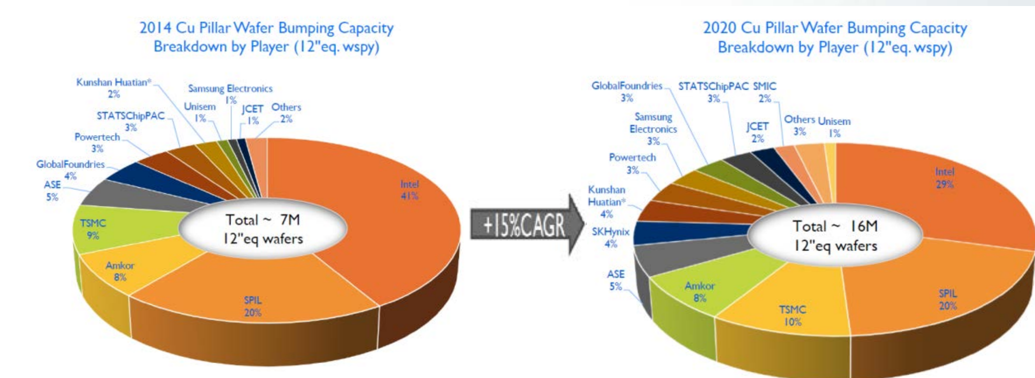


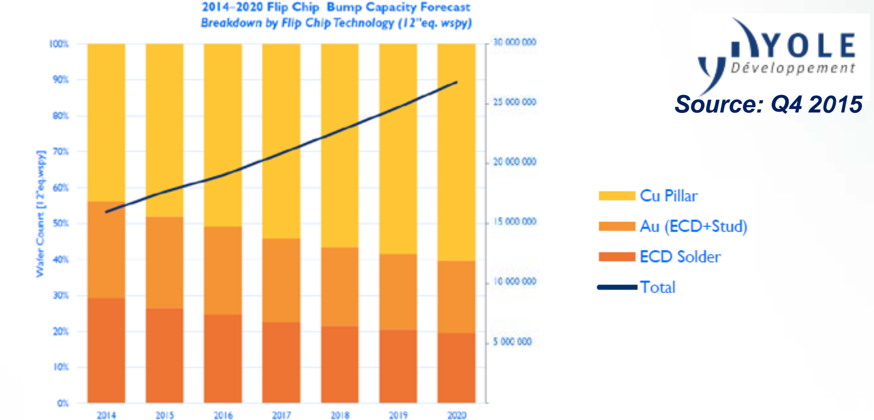
CuPillar w/wo Solder Cap

Market Overview

Flip Chip Packaging Trend – CuPillar will Take Major Market Share

- Wafer capacity forecast increase from 16M (2014) to 26M (2020)
- CuPillar wafer bumping capacity increase from 7M (2014) to 16M (2020)
  - CuPillar market expect to grow at CAGR(2014-20) of 15%
  - > 50% of bumped wafers for flip-chip are now CuPillar packages
  - Top 5 remain strong market position

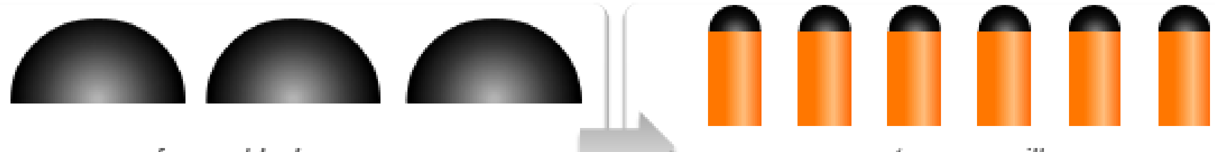




Source: Q4 2015

Market Overview
Why moving into CuPillar packaging

"Pillars" of copper are typically plated on the chip in wafer form through photolithography techniques. Solder bumps have fixed aspect ratios lower than one, whereas copper pillars offer aspect ratio flexibility, and therefore can increase I/O bump densities for many applications in addition to other advantages…



from solder bumps

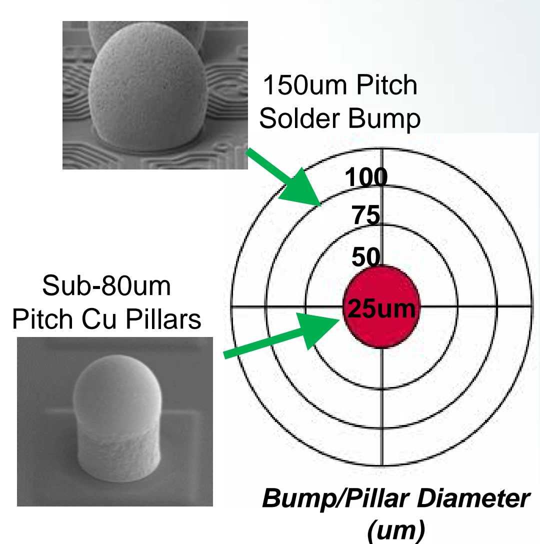
- Pitch limited to 150µm min, 120µm at best, due to spherical aspect and need for sufficient z-height gap for underfill flow
- Risks of electrical shorts by bridging
- Limited spacing between adjacent bumps for signal routing
- Limited spacing between adjacent bumps prevents the underfill from flowing causing underfill voids
- Reduced pitch leads to lower bump height (due to 1:1.3 aspect ratio) causing
  - Reliability issue by lack of bump elasticity
  - Reduced stand-off height making it more difficult for the underfill to flow.

to copper pillars

- Finer pitches possible down to 20µm
- Reduced risk of shorts between adjacent bumps
- Larger spacing between adjacent bumps for signal routing and easier underfill flow
- High bump aspect ratio (➔ easier underfill flow)
- Copper pillars are a reliable lead-free bumping option
- Copper offers higher electrical conductivity than solder: 25% lower resistance than SnPb
- Higher current density capability (better resistance to electromigration)
- But higher elastic modulus (stress during attach process)

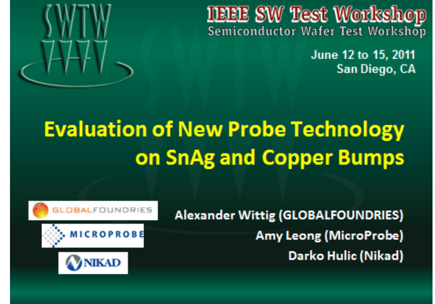
Market Overview
HVM CuPillar Probing Challenges

- **Probing on 3x smaller solder bump**
  - Require micron-meter level probe tip alignment control
  - Low vertical and lateral probe force for gentle touch down on small bump
- **Maintain High Probe Card Up-Time on HVM**
  - Increase current protection limit while probe is thinner
- **Probe Card Last through out the Product Life**
  - Longer life-time probe required while probe tip size is reducing



FFI Cu Pillar Probing Solution Evolution

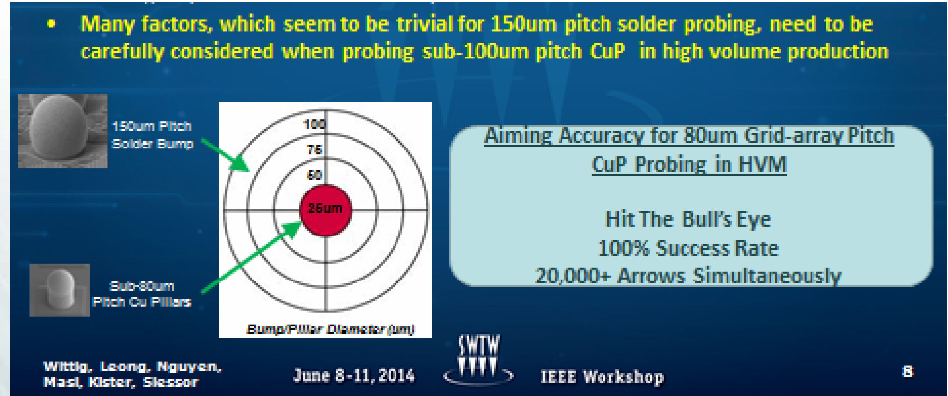
Started with 3mil, followed by 2.5mil, then MEMS for 100um Pitch and Below



2011: 150um Pitch
Cu Pillar Probing

2012: 120um Pitch
Cu Pillar Probing

2013: 100um Pitch
Cu Pillar Probing



MEMS Fabricated Vertical Probe Card for CuPillar Probing

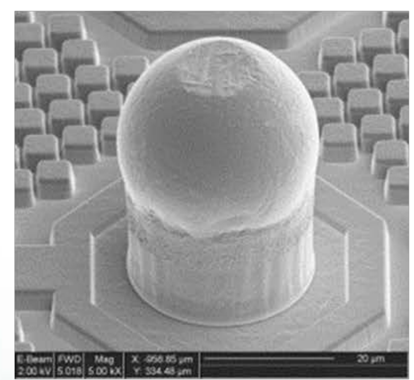
- Features Required for Fine Pitch CuPillar Probing
  - Fine Pitch, 40um for TSV or Si Interposer Probing, 60/80um CuPillar Production Probing
  - Low CRES, “No float” architecture for contact stability and thermal agility over wide temperature range
  - High current capability, 1.5 A/probe CCC
  - Long Life Time, Wear-resistive tip materials and geometries, ~ 2X longer lifetime vs. vertical at comparable bump pitch
  - HVM Capability, Machine-assembled probe head for high throughput and superior quality, >30k pins per card

Composite MF80 MEMS Probe with different materials, at different locations, with micron-level precision

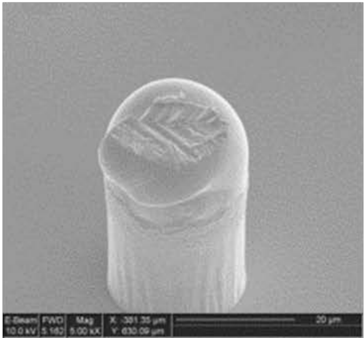
80um Pitch Grid-array MEMS Probe Head 30k pins, X8

CuPillar Probe Mark Photo Gallery

Aiming accuracy and probe force are essentials to get good probe mark

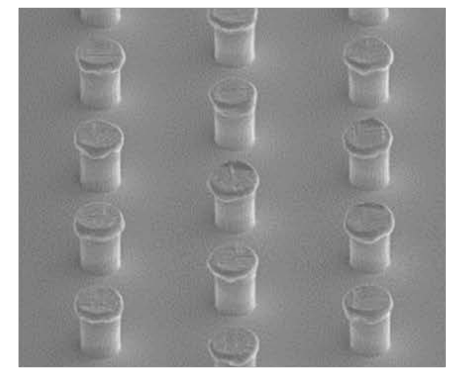


Pass
Good Probe Mark on 30µm Cu Pillar



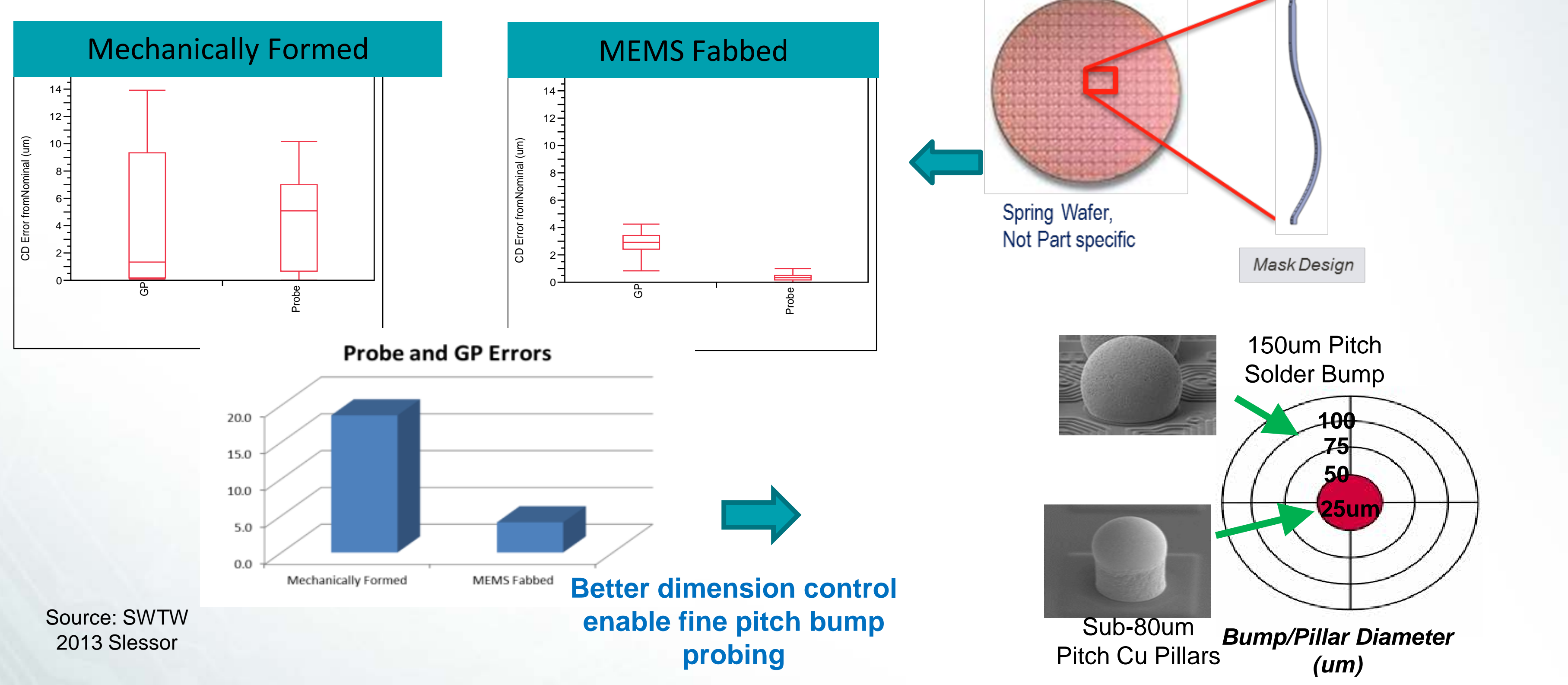
No Pass
Cu Pillars with Sheared Solder Cap

No Pass
Misaligned Probe Tip



No Pass
Probe force too high

Dimensional Control Improved With MEMS Fabrication Processes



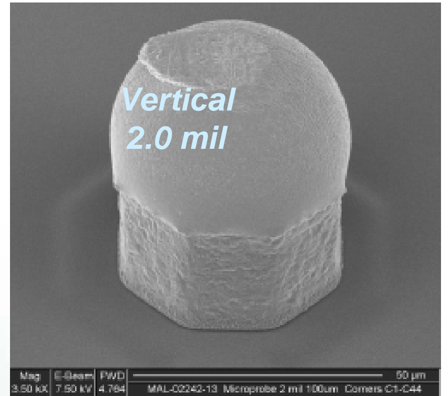
Source: SWTW 2013 Slessor

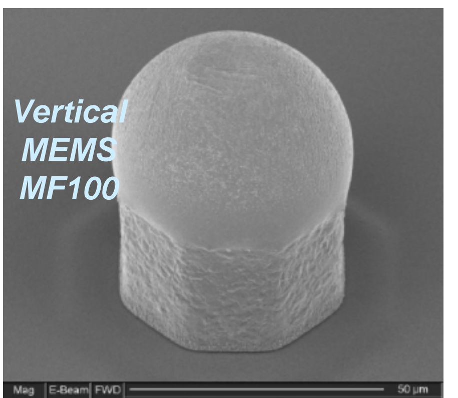
Better dimension control enable fine pitch bump probing

Low Vertical & Lateral Probe Force is Essential

Minimize CuPillar Impact, Better on Packaging Reliability

- Benefit of low-impact probing by MEMS Vertical Probe
  - Minimizes solder material displacement on the solder surface
  - Eliminate the need for additional reflow post wafer probing (due to solder damage)
  - More even force at pillar footing for better packaging reliability



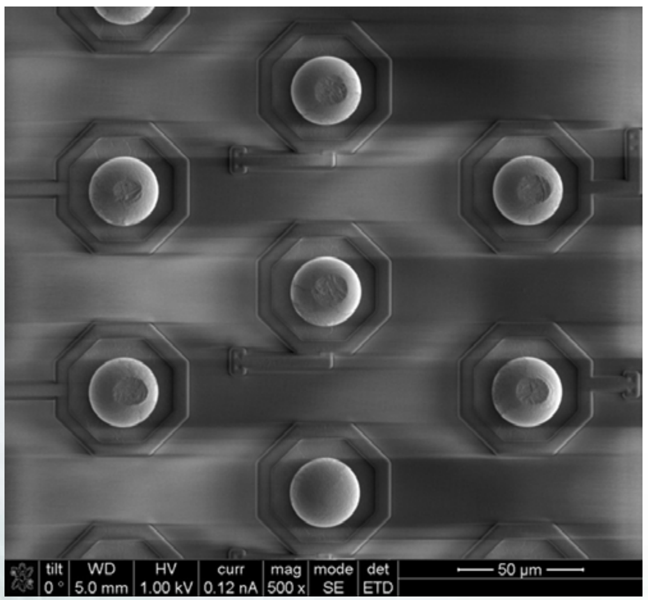


Probe Mark Comparison of Vertical MEMS MF100 vs. Vertical 2.0mil

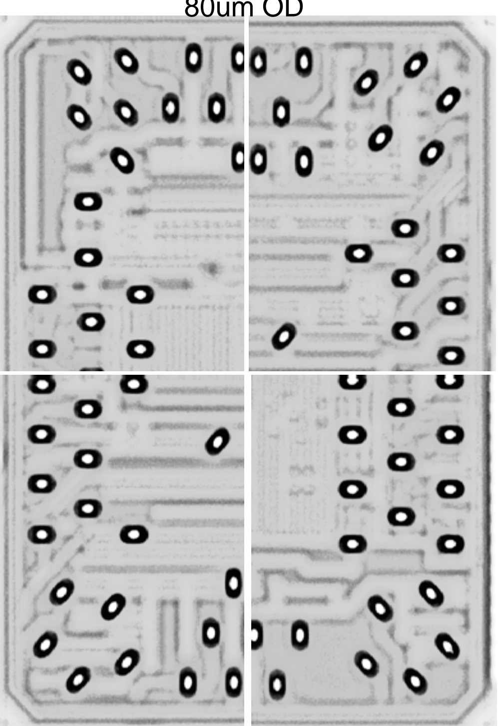
MEMS Vertical Probe Mark on 80um Pitch CuPillar

Hot Temperature at 90ºC

25um Cu Pillars
Probe Mark at 75um OT



Cu Pillar Size: 96umx59um
Probe Mark Size: 16um x 26um
80um OD

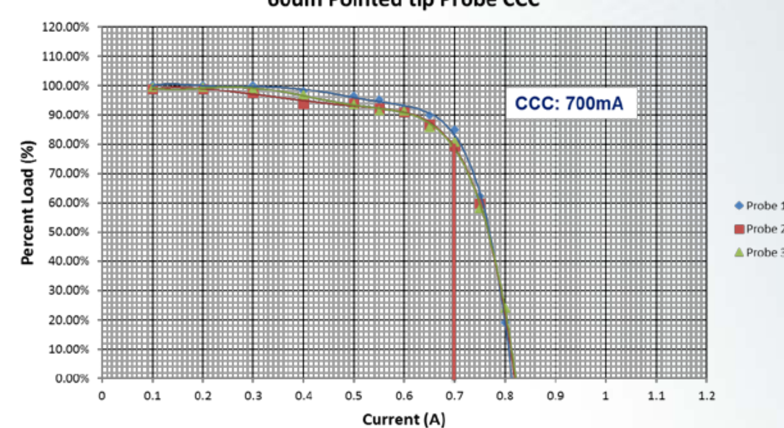


At max 125um OD Probe Mark still within 25%

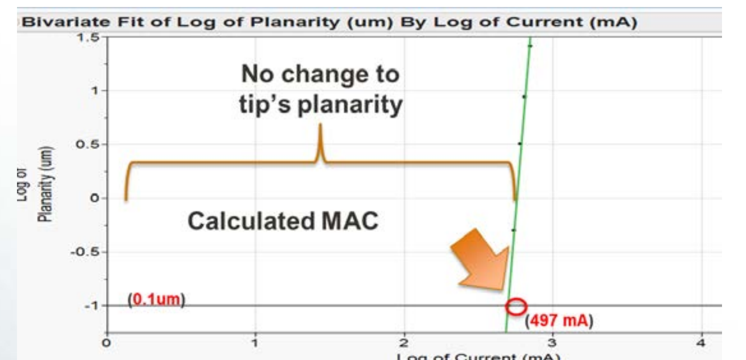
OD(OD1+?)	TD=?	P/M size X(um)	P/M size Y(um)	P/M(%)	P/M < 25%
OD1+70	TD=4	18	21	11.40%	Y
OD1+80	TD=4	16	24	11.60%	Y
OD1+90	TD=4	17	23	11.80%	Y
OD1+100	TD=4	17	26	13.30%	Y
OD1+110	TD=4	16	27	13.00%	Y
OD1+120	TD=4	17	27	13.80%	Y
OD1+125	TD=4	18	28	15.20%	Y
OD1+70	TD=6	17	25	12.80%	Y
OD1+80	TD=6	16	26	12.50%	Y
OD1+90	TD=6	17	27	13.80%	Y
OD1+100	TD=6	18	27	14.70%	Y
OD1+110	TD=6	17	28	14.40%	Y
OD1+120	TD=6	18	28	15.20%	Y
OD1+125	TD=6	18	29	15.70%	Y

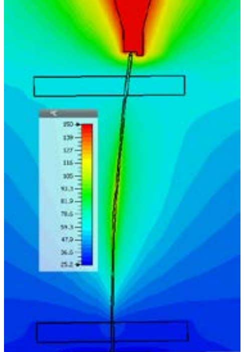
Current Carry Capacity Case Study

- Current Carrying Capacity (CCC)
  - ISMI CCC: 700mA (at Room Temperature)
  - Simulated CCC: 600mA (at 150ºC)
  - **ISMI CCC is the current where the spring force is reduced by 20%, current duty cycle 2min on and 2min off**

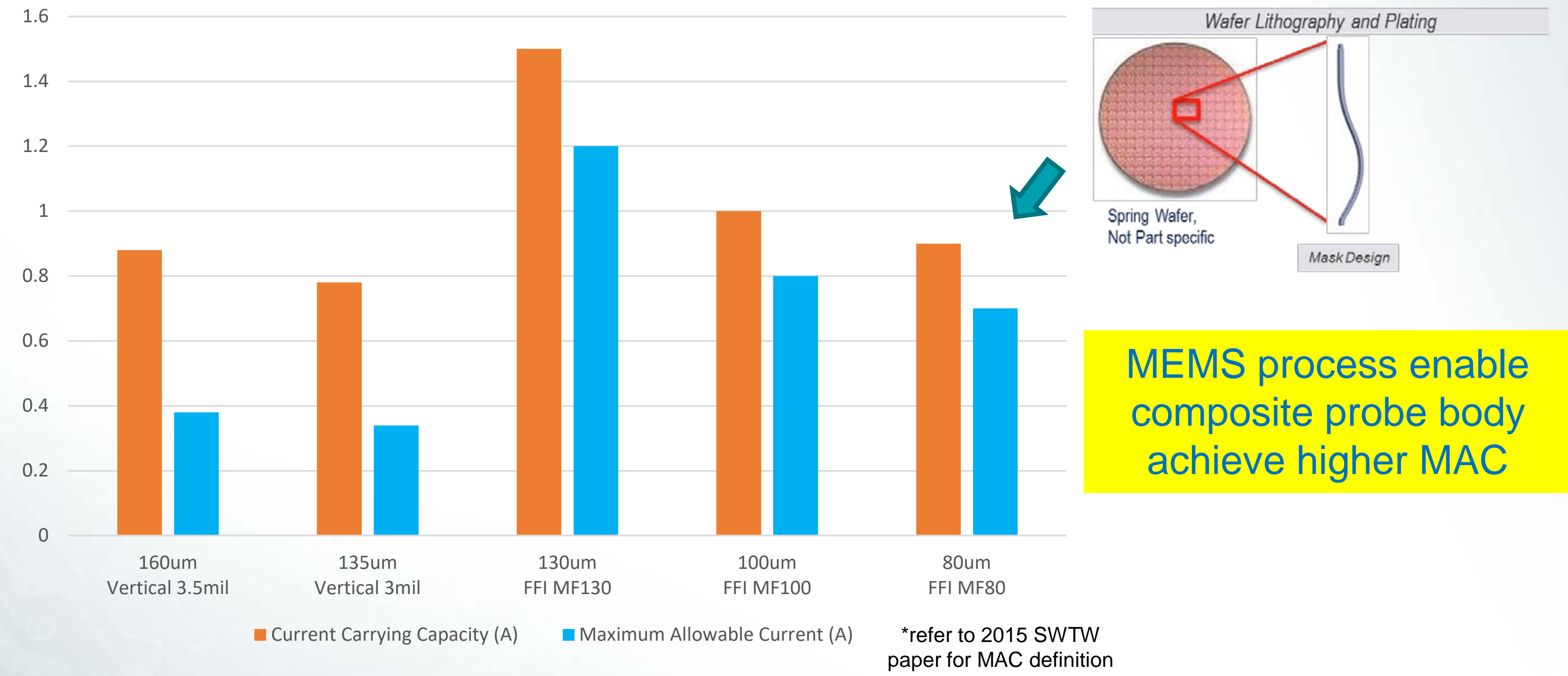


- Maximum Allowable Current (MAC)
  - MAC 500mA (at Room Temperature)
  - **Calculated current associated with a 0.1um change in planarity, current duty cycle 1min on and 1sec off**

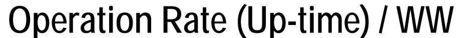




MEMS Probe Provides 2x Current Protection



Higher MAC, Less Burnt Probe Event Occur
PC Always Stay at Production Line

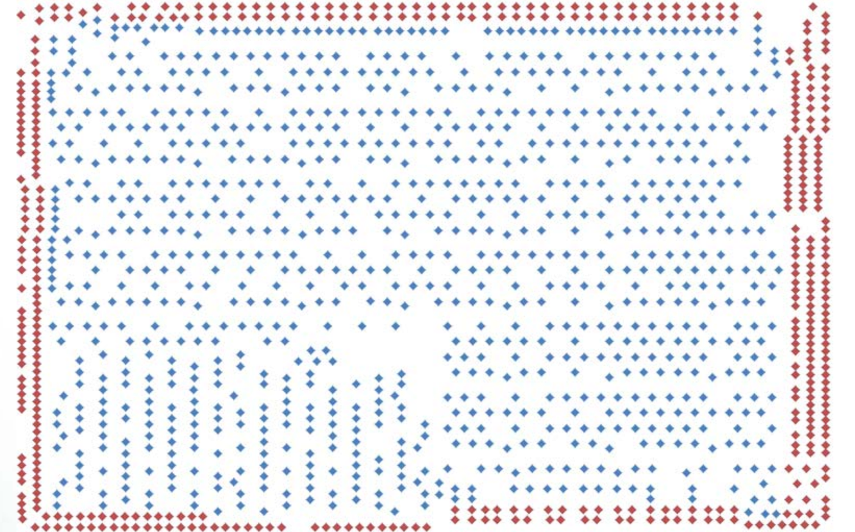


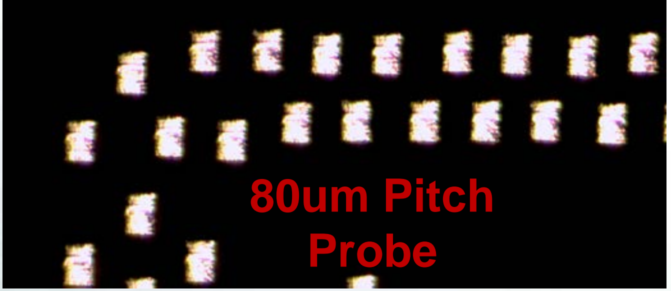
[%]

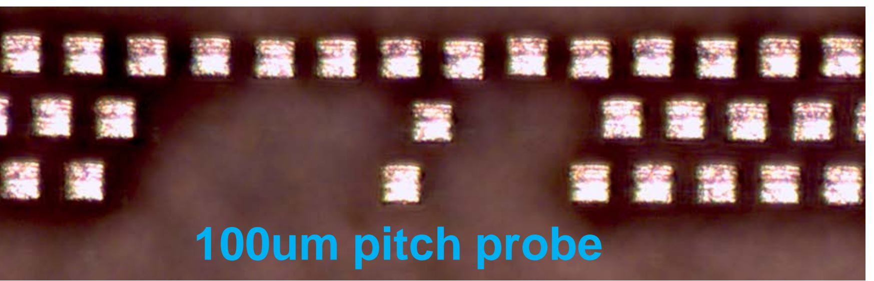
	ww 01	ww 02	ww 03	ww 04	ww 05	ww 06	ww 07	ww 08	ww 09	ww 10	ww 11	ww 12	ww 13	ww 14
Operation Rate [%]	89.8	90.5	85.1	90.1	95.2	98.7	97.4	97.0	99.6	95.7	99.6	100.0	100.0	98.7

	ww 15	ww 16	ww 17	ww 18	ww 19	ww 20	ww 21	ww 22	ww 23	ww 24	ww 25	ww 26	ww 27	ww 28
Operation Rate [%]	96.1	98.3	98.7	98.7	95.2	91.3	90.9	91.9	93.5	91.9	94.0	93.7	89.7	93.7

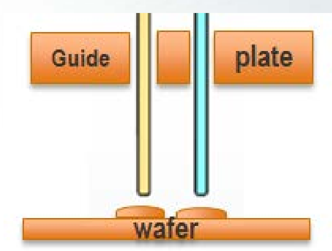
Optimize the Probe Selection for Best Performance







Vertical MEMS Probe Life-time Projection



- Vertical MEMS Probe Lifetime is a function of
  - **Tip Length** – How long is the usable tip length?
    - The longer, the better. However…
    - The longer, the worse aiming accuracy -> higher chance for misalignment or bump damage
    - Need to consider optimal tip length for targeted application for production stability
  - **Wear Rate** – How fast will the tip wear?
    - Dependent on tip material, probe design, cleaning media/routines
    - Traditionally no strong dependency for Cobra-style 3mil or 4mil, similar material/design
    - "Smart" MEMS probe design can significantly slow down the tip wear rate
  - **Cleaning Frequency** – How often does the probe tip need to be cleaned to maintain yield stability?
    - How sensitive is the device yield to Cres? How the tip material interact with probed pads/bumps?
    - Need to be validated on custom wafers to ensure production yield stability
- "Pure Clean" Lifetime Projection
  - **This is the lifetime if only cycling on cleaning media without solder accumulation**
  - **PureClean Lifetime = (([Tip length] / [wear per 1k cTD]*1000) / [#insertions]) * [CleaningInterval]**

Tip Size/Material Impact Life-time

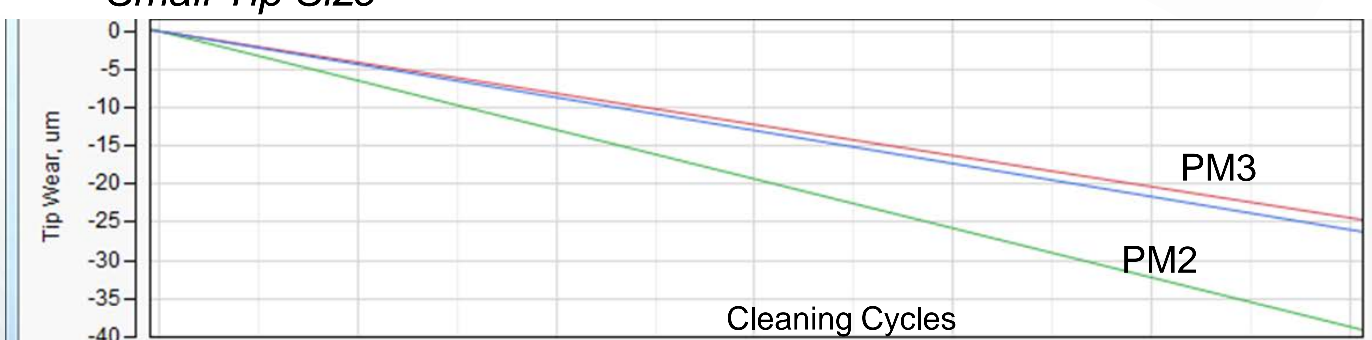
中國墨條 Ink Bar

Soft material
Small Tip Size

Which one of these bars will wear out at a faster rate on sand paper?

Stainless Steel Bar

Hard material
Large Tip Size



PM3 has 1.6x lifetime compared to PM2, assuming everything else is the same (product architecture, tip size, probe force, etc)

Continuously Extend Probe Life-Time
with new probe alloy and optimize probe tip dimension

Projected Lifetime (TD's)

1,600,000
1,400,000
1,200,000
1,000,000
800,000
600,000
400,000
200,000
0

MF100-HCCC
MF80-HCCC
MF100 — PM2
MF80-LL — PM3
MF80-LLX — Extended tip length

1st Generation Vertical MEMS Probe (MF100-HCCC, MF80-HCCC, MF100)

Current Generation (MF80-LL)

Future Generation (MF80-LLX)

MEMS Vertical Probe Life-time Study
Projected Life-time Close to 1M Touch Down

- High-end mobile application processor x8 design, total ~30K probes
- MF80-LL on probing 80um Pitch CuPillar with solder cap
- Total 26 cards shipped
- Data collected by customer with 6 different cards

Projected Lifetime TD's
Current TD's

TD's Count

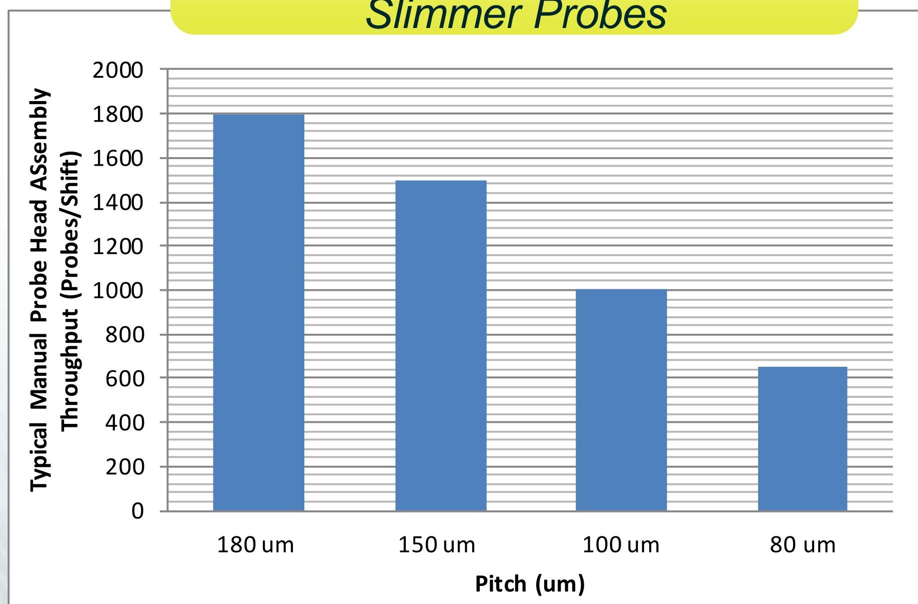
1000000
900000
800000
700000
600000
500000
400000
300000
200000
100000
0

#04 #06 #12 #16 #19 #23

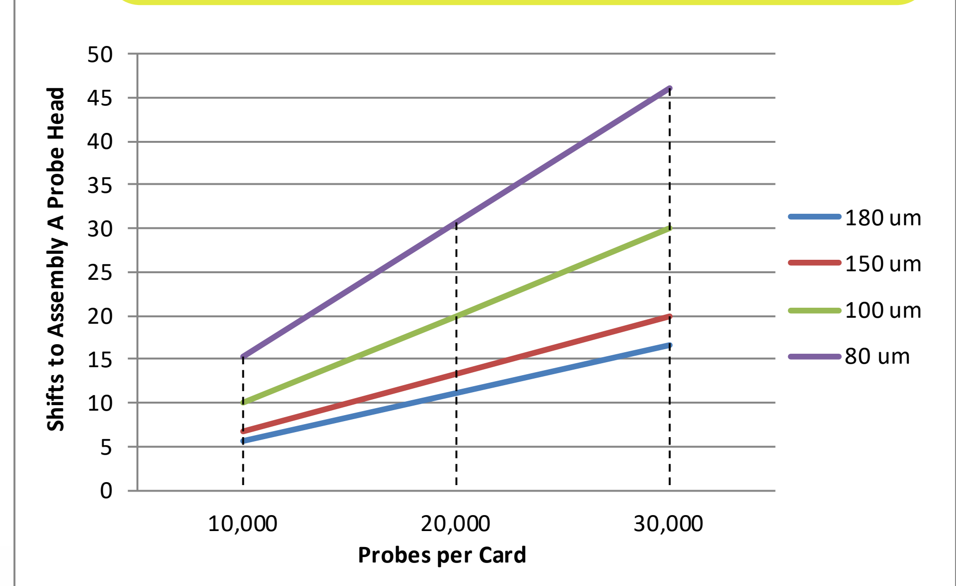
Probe Card ID

Probe Assembly Throughput Is Becoming An Issue for Probe Card Cycle-time @ 80um CuPillar Pitch

Vertical Probe Assembly Throughput Decreases with Slimmer Probes



Probe Head Assembly Is Becoming the Critical Path to Probe Card Cycle-time As Pin Counts/Probe Card Approaches 20k Pins

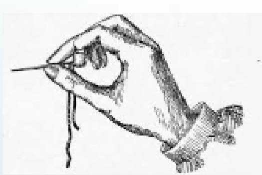


Time-to-Volume Ramp-up @ 80um CuPillar Pitch
What if 10 cards are needed in a week to address peak demand?

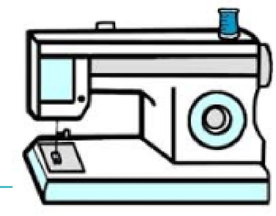
Pitch	5 Cards/Wk	10 Cards/Wk
180 um		
150 um		
100 um		
80 um		

Concurrent Assembler Shifts (y-axis: -, 10.00, 20.00, 30.00, 40.00, 50.00, 60.00, 70.00, 80.00, 90.00, 100.00)

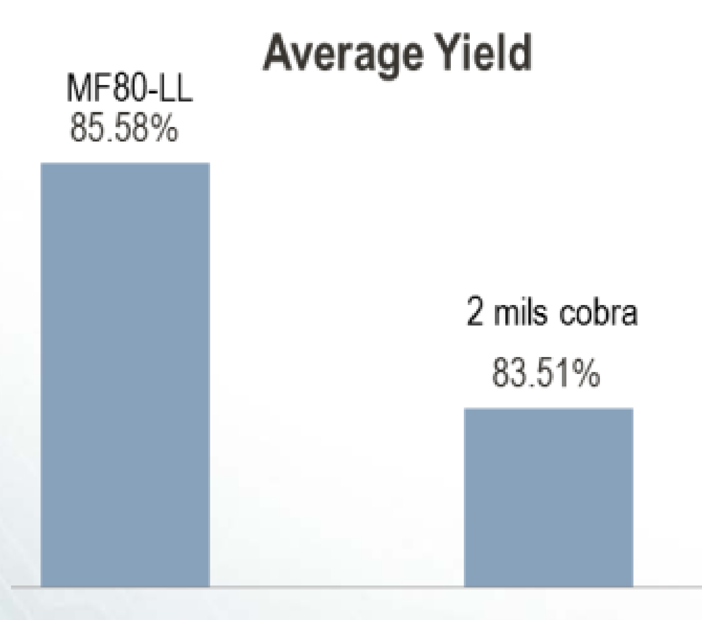
With manual probe head assembly, to ship 10 units of 30k-pins 80um-pitch probe cards in a week, ~100 concurrent assembler shifts are required!!!

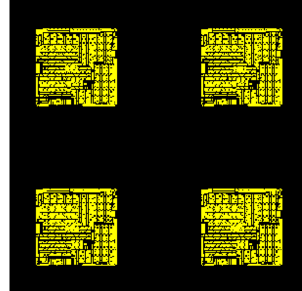


"Hand to Machine" Conversion on MEMS Vertical Probes



MEMS vs. Conventional 2mil CuPillar Wafer Probing Yield Comparison





- Project Background
  - MEMS 80um pitch and Conventional 2mils probe were used to compare yield on a mobile SoC design
  - 85um pitch, 4-DUTs, 9k pins, 45x100um Oval-shape CuPillars
- Results
  - MEMS Probe Head showed ~2.07% yield higher than conventional probe head
  - Measured on customer site 3 Lot total 75 wafers.

MEMS Technology Adoption in Advanced PC Market

- Total Advanced Probe Card Market continue growing to 2021
  - CAGR (2016~21) 6.4%

- MEMS Probe Card contribute most market growth
  - VLSI forecast MEMS PC market maintain CAGR (2016~21) 10.2%
  - MEMS PC revenue surpass conventional vertical PC revenue since 2016

Foundry and Logic Advanced PC Market

Source: VLSI Research

$1,000
$900
$800
$700
$600
$500
$400
$300
$200
$100
$-

$117
$145
$178
$213
$308
$342

2012
2013
2014
2015
2016
2017

Conventional Vertical Probe Cards
Other Advanced Probe Cards (RF)
MEMS Probe Cards

MEMS Technology for Fine Pitch CuP & Advanced Packaging Testing

Packaging Pitch	250-500um	135 – 245um	80 – 130 um	40 - 50 um
	WLP	BGA	Cu Pillar	TSV
Wafer Packaging				
FFI Solution	QiLin™ Vertical Spring Pins	Apollo™ Vertical	Apollo™ & Vx™ Vertical MEMS	Vertical MEMS

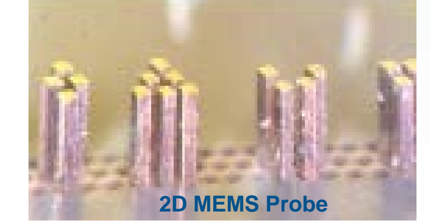
FormFactor Probe Card Product Portfolio

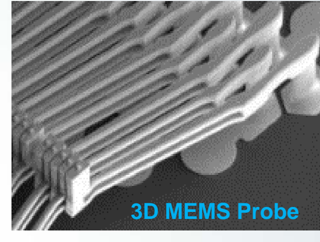
Addressing a Wide Range of Test Cost and Application Requirements

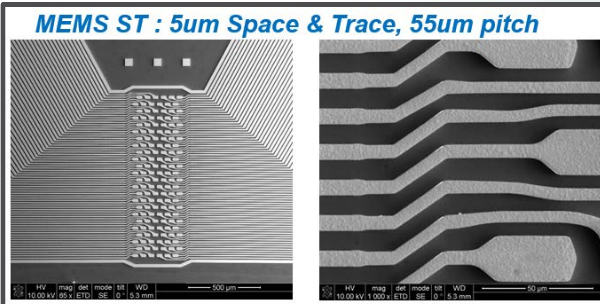
FormFactor™

FormFactor/Cascade Combined Technologies
Enabling Next-generation IC Test Challenges

- World largest MEMS fab for probe card application
  - 2D MEMS, 40 & 30um pitch solution for wafer & **2D+ PKG/TSV** test
  - 3D MEMS, new material capable >175C for **automotive & high temp** test
  - RF MEMS, low inductance and 50Ωn impedance probe for **HF 5G application**
  - Fine pitch Space Transformer, MLO or MLC, Metalized Guide Plate

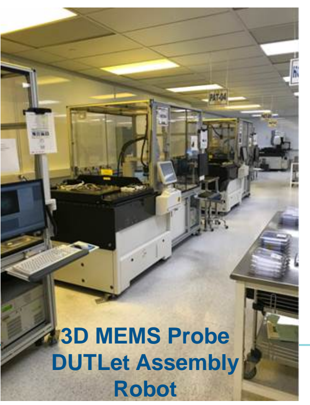

2D MEMS Probe


3D MEMS Probe


MEMS ST : 5um Space & Trace, 55um pitch

- ROBOTIC CAPABILITY
  - Fully-automated 2D probe assembly capability
  - DUTlet assembly at micron-level precision in x/y/z
- DESIGN AUTOMATION
  - Touchdown optimization (TDO) and Total Cost of Test (TCoO) Analysis
  - Advanced Tester Resource Extension (ATRE), ie. Power resource splitter
  - Tester channel to DUT channel assignment optimization
- ENGINEERING SYSTEM CAPABILITY
  - CM300xi for singulated die testing on carrier
  - Estrada-EM for TSV electro-migration defect detection and measurements

Custom IC


3D MEMS Probe DUTLet Assembly Robot

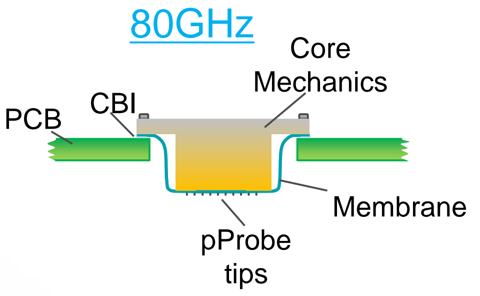
Fully-Automated 2D MEMS Probe Assembly Robot

Production Probe Card for Radio Frequency Testing

Cover from 5GHz to 80GHz

pProbe Probe Card

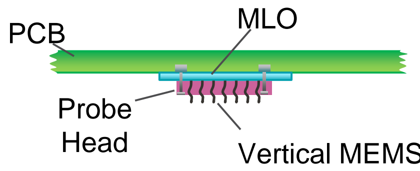
80GHz



- RF Performance: >80GHz ☆
- Space Transformer: Membrane
- Max Area: 10 x 38mm
- Common PCB: Possible ☆
- Pin Repair: No
- Pin-Pin Compliance: +/-20um
- NPI Leadtime: 5-8 weeks ☆
- Status: Released to Production

Katana-RF Probe Card

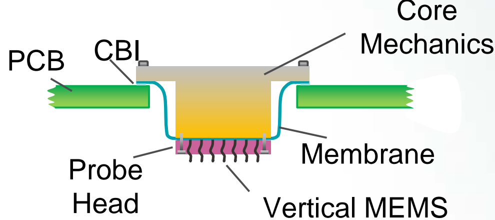
High Parallelism



- RF Performance: <10 GHz
- Space Transformer: MLO
- Max Area: ~75 x 75mm ☆
- Common PCB: No
- Pin Repair: Yes ☆
- Pin-Pin Compliance: +/-100um ☆
- NPI Leadtime: 8-12 weeks
- Status: Released to Production

Pyrana Probe Card

Common PCB

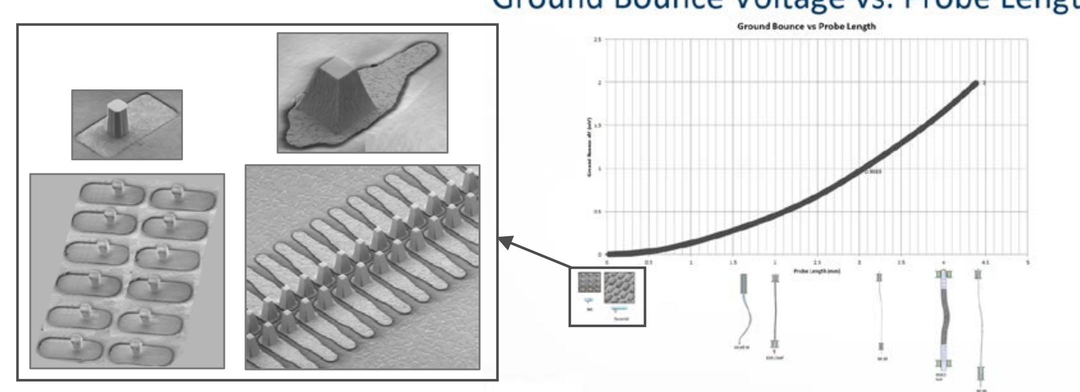


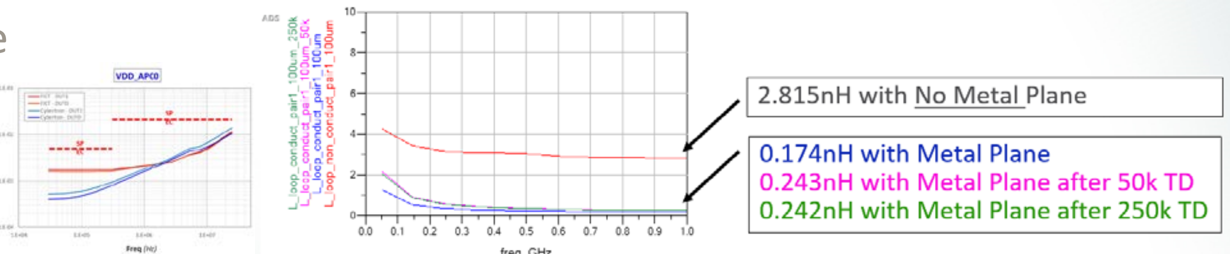
- RF Performance: <10 GHz
- Space Transformer: Membrane
- Max Area: 10 x 75mm
- Common PCB: Yes ☆
- Pin Repair: Yes ☆
- Pin-Pin Compliance: +/-100um ☆
- NPI Leadtime: 6-9 weeks ☆
- Status: In Pilot

**CBI: interface from membrane to PCB, common PCB to support multiple probe heads*

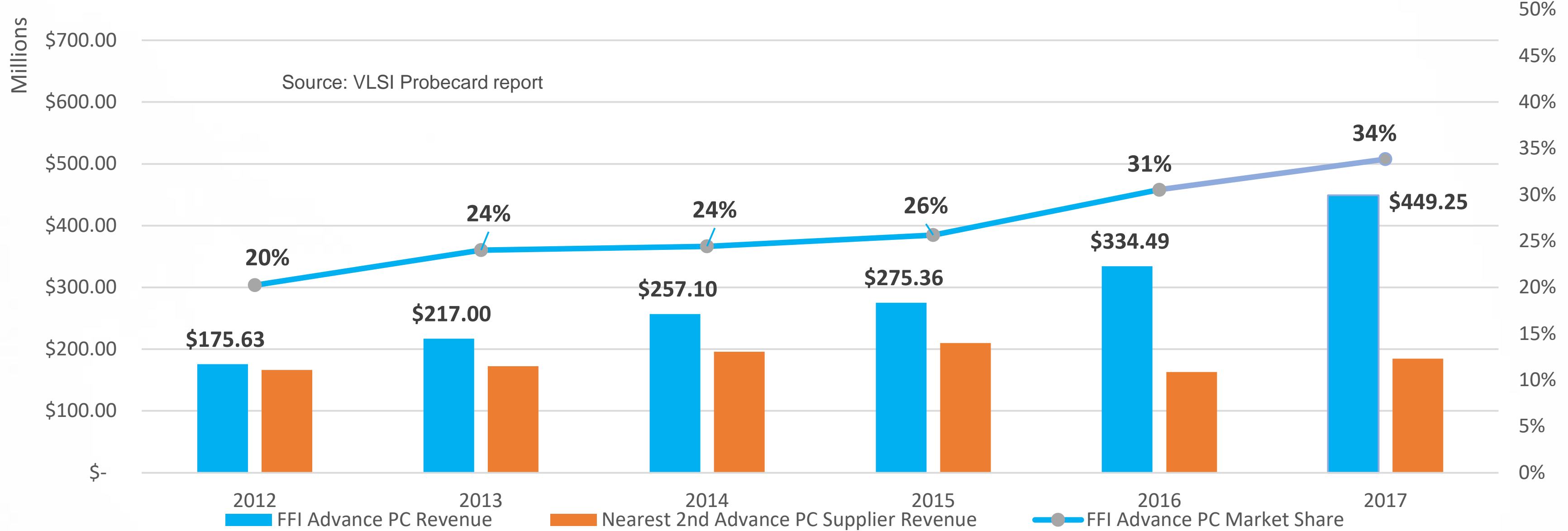
R&D Focus – High Frequency/PDN in Wafer Test

- Enable Wafer Test results Equivalent to Package Test Performance
- Approach: Low inductance probes, Innovating probe shielding
  - Short probe length, 200um
  - Metalized GPs
  - 50 Ohm Impedance probe





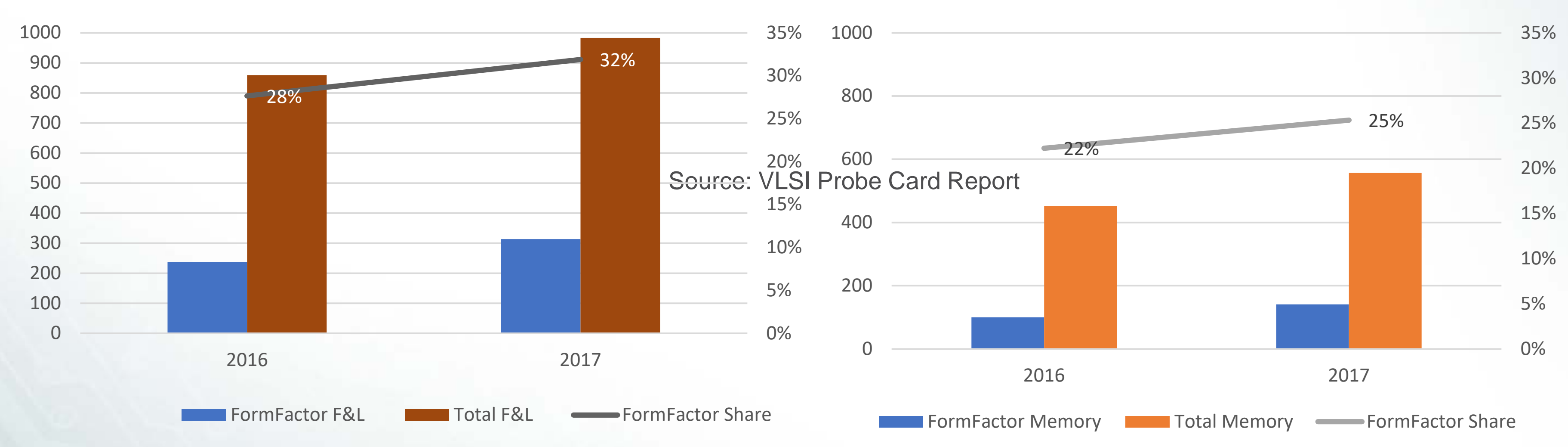
FormFactor's Leadership in Advanced Probe Cards



- FormFactor is the **#1** Advanced Probe Card Supplier
- Consistently growing market share leadership 6 years in the row
- Continued R&D and Support investments to innovate and enable smooth production

FormFactor #1 Logic and Foundry Probe Card Supplier

- Logic and Foundry Probe Card Market:
  - 2017 total logic and foundry PC market ~$984M
  - Formfactor #1 market share at 32%, fastest growing in 2017 by ~$76M

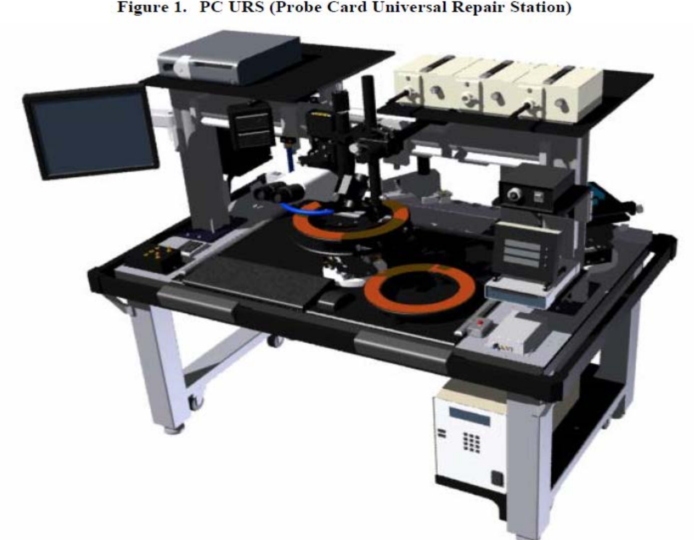


FormFactor China

- Founded in 2006, about 80 employees
- $1.5M investment to expand capacity & service capability in China
- Suzhou open house in September 2016– “10 Years and Counting”

Advanced Tooling Capability

- URS,PRVX3, PRVX4(the 1st advanced probe card test system in China), DD sanding station and metrology tool in place



Conclusion

- **Static trend of SoC flip chip packaging technology is moving into CuPillar**
  - In 2016 >50% of wafer bumping with CuPillar package
  - CuPillar market expect to grow at CAGR of 15% through out 2020
- **Conventional probe technology reaches its limitation on testing fine pitch CuPillar**
  - Alignment accuracy, probe force, current carrying capability
- **MEMS probe technology is required for fine pitch CuPillar HVM testing**
  - Micro-meter level probe tip aiming accuracy
  - Low 3D probe force
  - Higher maximum allowable current
  - Lower probe tip ware-out rate
  - High throughput and superior quality