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Automated Testing of Bare Die-to-Die Stacks*

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Abstract

Stacking singulated dies is an efficient way to create die stacks; IMEC uses this so-called die-to-die (D2D) stacking approach often to manufacture small to medium volumes of test chips. There is a need to perform a post-bond test on still-unpackaged (*'bare'*) D2D stacks, if only to avoid unnecessary packaging costs. This paper presents an approach to perform automatic stepping and probing on arrays of D2D stacks pick-n-placed (PnP'd) on a carrier substrate. We describe an algorithm for Cascade Microtech's CM300 probe station to automatically correct small PnP misalignments. Subsequently we present experimental results for PnP'd D2D stacks on three types of carriers: (1) dicing tape on tape frames for ⌀100mm wafers, (2) sheets of single-sided thermal-release tape, and (3) ⌀300mm carrier wafers with double-sided thermal-release tape. Finally, we describe adaptations to the CM300 probe station to be able to handle 400mm-wide tape frames for ⌀300mm wafers.

1 Introduction

There is a lot of excitement around and expectations from 2.5D- and 3D-stacked integrated circuits [1]. In 2.5D-SICs, multiple active dies are placed side-by-side on top of and interconnected by a passive interposer die. In 3D-SICs, multiple active dies are stacked vertically. Both 2.5D- and 3D-SICs are enabled by the ability to manufacture high-density arrays of small micro-bumps that electrically connect two stacked dies, and through-silicon vias (TSVs) that provide an electrical connection between the front- and back-side of a silicon substrate [2–4]. In 2.5D-SICs, TSVs connect the stacked active dies through the silicon interposer to the package substrate. In 3D-SICs, TSVs provide vertical interconnections between the various stacked dies. Both types of SICs serve their particular market segments and are here to stay; 2.5D-SICs provide better chip cooling options and hence typically target high-performance computing and networking applications, whereas 3D-SICs with their small footprint are better suited for mobile applications.

We distinguish three principal ways to create die stacks: (1) die-to-die (D2D), (2) die-to-wafer (D2W), and (3) wafer-to-wafer (W2W) [5]. All three methods have their specific benefits and drawbacks. In this paper, we focus on D2D stacking. Benefits of D2D stacking include that it allows to stack dies of different sizes on top of each other, and to select and stack only dies that passed a pre-bond test, thereby significantly enhancing the compound stack yield. For these reasons, D2D stacking provides an efficient way to generate stacking results and hence is often utilized for research test chips at IMEC. Figure 1 shows a collection of D2D-stacked 2.5D- and 3D-SIC test chip examples produced at IMEC.

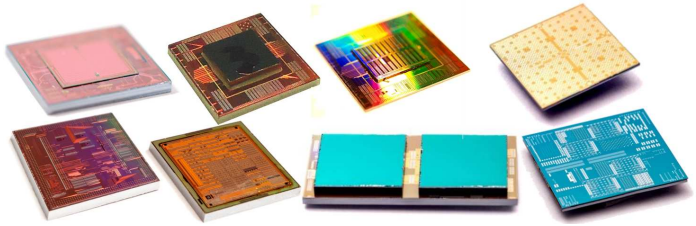

Figure 1: Examples of D2D-stacked 2.5D- and 3D-SIC test chips at IMEC.

One of the drawbacks of D2D stacking is related to the individual handling of the singulated die stacks. Traditionally, D2D stacks are transported in 'waffle packs': trays (typically made out of plastic) with cavities at the size of the die stacks, where the D2D stacks are placed in (see Figure 2). During transportation itself, the die stacks are held in place by the waffle pack and its lid, but when they need to be handled, the waffle pack's lid needs to be lifted and the D2D stacks are at risk to fall out of the waffle pack.

Figure 2: Example waffle pack, here holding eight singulated dies.

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One of the occasions when D2D stacks need to be handled is when their post-bond test is applied, i.e., testing the still-unpackaged ('bare') die stacks. Post-bond testing is useful to check whether the stacking operation was successful (i.e., if the inter-die interconnections work) and whether the intra-die circuitry has survived the thermo-compression stacking operation. Die stacks which fail the post-bond test do not need to be packaged. We have two options for post-bond test probing.

1. *Per-stack placement on the probe station.*
   The D2D stacks need to be lifted from the waffle pack and placed on the probe station's chuck (see Figure 3) and vice versa. At IMEC, this was a manual process, with the risk of die stacks falling out of the waffle pack and potentially getting damaged and/or losing the identification and tracking of individual stacks. Also, the per-stack probe-to-pad alignment on the probe station required engineering presence and became a true bottleneck in test throughput.

Figure 3: Manually placed D2D stack on the auxiliary chuck of a CM300 probe station.

2. *Stacks in bare-die tray.*
   A collection of D2D stacks can be put on the probe station's chuck in a bare-die tray. There exist commercially available trays which are customized for a particular die size. These trays distribute the chuck's vacuum to each die position in the tray, in order to hold the dies (or die stacks) in a fixed position during probing. This vacuum distribution network makes these trays too expensive to also serve as transportation means. Consequently, this approach requires transfer of the die stacks from the original waffle pack into the tray before testing and vice versa afterwards; at IMEC, this operation was manual, with all associated risks of die stacks falling out of the waffle pack and/or bare-die tray and potentially getting damaged, and/or losing the identification and tracking of individual stacks. This approach also requires time-consuming per-stack probe-to-pad alignment, as the relative positions of dies/die stacks in the tray will not be identical.

In this paper, we set out to improve the post-bond test efficiency for bare D2D stacks by probing on arrays of D2D stacks PnP'd on a carrier substrate, instead of on single D2D stacks. Loading such a carrier substrate onto the probe station implies loading many D2D stacks simultaneously. The D2D stack array structure allows for automatic index stepping and probing by the probe station, provided that it can automatically correct small PnP-induced misalignments. Furthermore, the carrier substrate might be usable as transportation vehicle to downstream operations, such as packaging by an OSAT company.

This paper describes an algorithm that allows Cascade Microtech's CM300 probe station to automatically correct small misalignments, using the CM300's built-in *'AlignChip'* routine. Subsequently, we present experimental results for arrays of IMEC D2D stacks PnP'd on three different types of carriers: (1) dicing tape on tape frames for ⌀100mm wafers, (2) sheets of single-sided thermal-release (TR) tape, and (3) ⌀300mm carrier wafers with double-sided thermal-release tape. Finally, we describe adaptations to the CM300 probe station to enable loading of 400mm-wide tape frames for ⌀300mm wafers.

The remainder of this paper is organized as follows. Section 2 details the automated misalignment correction algorithm that we have implemented on Cascade Microtech's CM300 probe station. Sections 3 and 4 describe respectively our experimental set-up and results. Section 5 describes a recent extension to the CM300 prober to handle large tape frames for ⌀300mm wafers. Section 6 concludes this paper.

2 Misalignment Correction Algorithm

This section describes the automatic re-align procedure that we have implemented on the CM300 probe station (see Figure 4) at IMEC. This modular probe station consists of two independent probers (left and right) and a shared Material Handling Unit (MHU) in the middle. Single wafers or tape frames can be loaded manually via the front-side load doors on each prober. Alternatively, ⌀300mm wafers can also be loaded automatically from the wafer cassette load ports on the MHU onto either prober.

Figure 4: CM300 automatic probe station in dual cluster configuration.

The probe station has four software-controlled degrees of freedom for chuck movement: translations x_c, y_c, and z_c, and rotation θ_c. Any translation of the die stack in x_s, y_s, and/or z_s direction can be compensated by translating the chuck. As shown in Figure 5, a rotational misalignment θ_s is a rotation around the center of the die stack, whereas the compensation θ_c is a rotation around the center of the chuck. Therefore, limited rotational

misalignments θ_s can be compensated by a combination of chuck translations (x_c, y_c) and rotation (θ_c), but if θ_s becomes too large, the prober's misalignment compensation becomes ineffective.

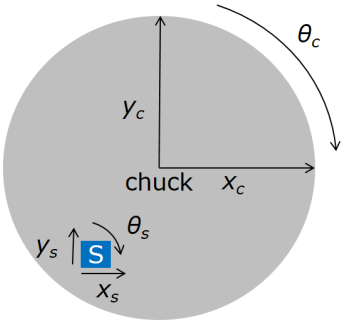


Figure 5: Translation and rotation misalignments and corresponding chuck compensation.

VeloxPro, the software system of the CM300 probe station, has three different re-align functions built in.

- `ReAlign 2 H`
  - Works per wafer; corrections in x, y, z, and θ
  - Meant to be used after loading a new wafer or temperature changes
- `ReAlign 2 C`
  - Works for every n^{th} die; corrections in x, y, and z
  - Meant for accuracy improvement on small probe pads
- `AlignChip`
  - Works per single die; corrections in x, y, z, and θ
  - Meant to be used for singulated dies and positioners

Given the fact that we wanted to correct PnP misalignments on individual die stacks, we used the *'AlignChip'* function.

The CM300 has four downward-looking cameras: eVue1, eVue2, eVue3 (all positioned on the microscope bridge), and the platen camera. Initially, we used *'AlignChip'* with the eVue1 camera. Later, we replaced this by the platen camera, which avoids the risk of collision with the probe card and still has a sufficiently large field-of-view (FoV), viz. $1.50\times1.10\text{mm}^2$. Alignment correction is possible as long as the trained alignment pattern is in the FoV of the camera used. In other words, the maximum misalignment that can be corrected automatically by the *'AlignChip'* function is the FoV size minus the size of the alignment pattern. In case the FoV is insufficient, the VeloxPro software has advanced options to enlarge the FoV by stepping around. Also, a second (back-up) alignment pattern can be defined.

Algorithm 1 [AUTOMATICREALIGN]

```
1: Step 1: SETUPPROJECT
2: for all carriers do {
3:     Step 2: MANUALOPERATION
4:     Step 3: AUTOMATEDOPERATION
5: }
```

The automatic re-align procedure is described in Algorithm 1 and contains three steps.

Step 1, SETUPPROJECT is executed once per project.

Step 1 [SETUPPROJECT]

```
1: Measure x, y index for STEPNEXTDIE
2: Training of ALIGNCHIP plug-in: pattern recognition and Home setting
3: Training of DETECTWAFERHEIGHT plug-in
4: Create "wafer" map:
5:     Maximum number of die stacks in x and y (e.g., 7×7)
6:     Input x, y index for STEPNEXTDIE as measured in Step 1.1
7:     Define coordinate system (e.g., origin (0, 0) is south-west die stack)
8:     Define probe route (e.g., snake bottom-up)
9: Load probe-card training model (or re-train probe card)
```

Step 2, MANUALOPERATION is the manual part of the algorithm which has to be repeated per carrier.

Step 2 [MANUALOPERATION]

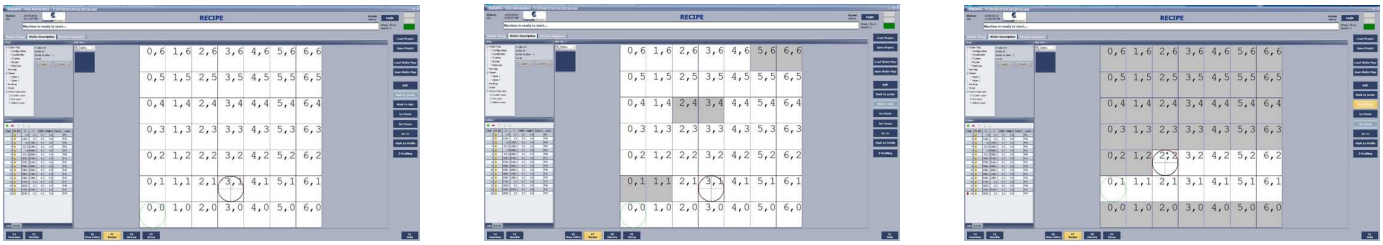
```
1: Place carrier on chuck with center die on center of chuck
2: Indicate in wafer map die stacks to-be-probed/skipped
3: Load chuck and move to platen camera
4: Move manually to (nearby) dicing street of center bottom die
5: ALIGN2POINT for first coarse alignment of carrier
6: Move manually to Home position on center die stack
```

Step 3, AUTOMATEDOPERATION is the part of the procedure which runs automatically in LabVIEW, and which has to be repeated per carrier.

Step 3 [AUTOMATEDOPERATION]

```
1: Perform ALIGNCHIP on center die
2: Perform DETECTWAFERHEIGHT
   % SynchronPosition is defined (by means of pattern recognition of cross
   % on chuck) and wafer height detection is performed on center die
3: for all stacks do {
4:     STEPNEXTDIE % First sub-die (0,0) is base to start ALIGNCHIP
5:     Move under platen camera
6:     ALIGNCHIP
7:     FINDFOCUS: invokes LabVIEW algorithm for calculation ContactHeight
8:     ALIGNCHIP % Second time, just to be sure
9:     Move to ProbePosition % Now perfectly aligned
10:    Set Home
11:    Prepare test: datafile headers, light off, init contact counter, etc.
12:    for all sub-dies do {
13:        Contact; measure; separate; write data to file
14:        STEPNEXTSUBDIE
15:    }
16: }
```

In Step 1.4, we define the 'wafer' map for the array of PnP'd die stacks. Fortunately, the CM300 software allows us to define rectangular 'wafer' maps (see Figure 6). Here we also input the size of the x and y index steps as measured in Step 1.1. For identification, we define a coordinate system; the convention is to use the south-west die stack as (0,0) origin. Finally, we need to define a probe route (for example, *'snake up'*). Additionally, per carrier we need to indicate in the 'wafer' map which die stacks need to be probed vs. which can be skipped; the latter are grayed out in the CM300 'wafer' map (see Figures 6(b) and 6(c)).



(a) Full array. (b) Some stacks skipped. (c) Most stacks skipped.

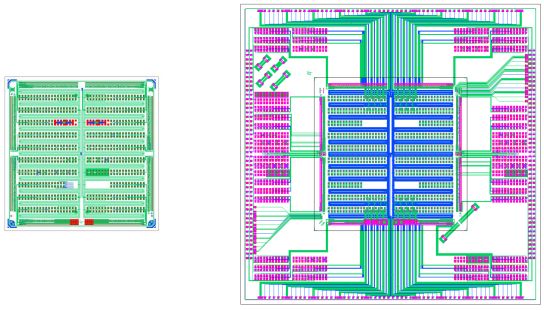
Figure 6: Example rectangular wafer maps for 7×7 array of PnP'd die stacks.

3 Experimental Set-Up

3.1 Stacked Test Chips

As test vehicle for our experiments, we used two IMEC 3D test chips, both containing two metal layers, micro-bumps of various sizes, and various other 3D test structures.

- PTCO: 5.2mm × 5.2mm (layout: see Figure 7(a)).
- PTCP: 10.2mm × 10.2mm (layout: see Figure 7(b)).



(a) PTCO. (b) PTCP.

Figure 7: Layouts of 3D test chips (a) PTCO and (b) PTCP.

These two dies are meant to be stacked as 3D-SICs, where PTCP serves as bottom die, on which up to four copies of PTCO dies can be stacked in a single center tower. In the experiments reported here, we worked with 3D-SICs consisting of one PTCO die stacked on top of one PTCP die, as shown in Figure 8.

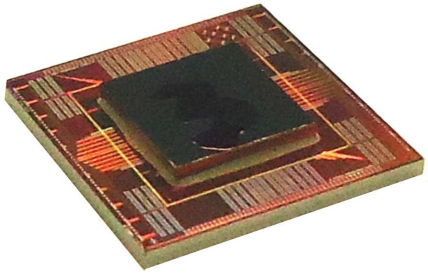


Figure 8: Photo of a single bare PTCO/P D2D stack.

Post-bond testing of the still-unpackaged (bare) PTCO/P stacks involves probing on multiple probe-pad modules. These probe-pad modules are all located on the front-side (= top-side) of the bottom PTCP die, in the part of the layout outside the center where the PTCO die is stacked. Each probe-pad module is IMEC's standard probe-pad module, as shown in Figure 9, consisting of 2×12 probe pads of 60μm × 80μm each at 100μm and 110μm pitch respectively.

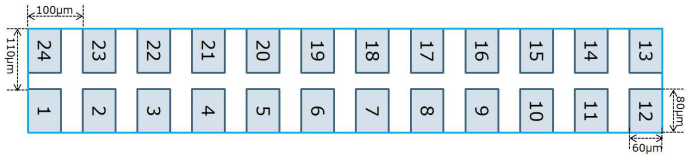


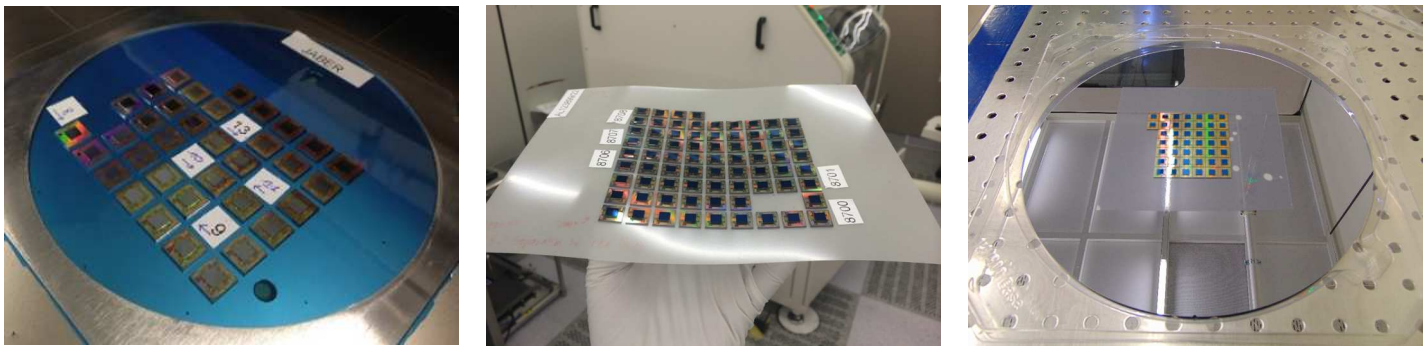
Figure 9: IMEC-standard 2×12 probe-pad module.

Probing these probe modules was done with a conventional cantilever probe card. The cantilever needles need to have extra-long probe tips, in order to compensate for the z height of the stacked PTCO die. The probe card has 2×12 needles, and hence multiple probe card touch-downs are required to cover the multiple probe-pad modules per die, i.e., with one probe card touch-down per probe-pad module.

3.2 Arrays of PnP'd Bare Stacks on Carrier

With a standard PnP tool, we populated arrays of bare PTCO/P D2D stacks on three types of carriers.

1. *Dicing tape on tape frames for ⌀100mm wafers.*
   The blue dicing tape was manually laminated onto the tape frames. PTCO/P D2D stacks were PnP'd in arrays of maximal 7×7=49 stacks per frame (see Figure 10(a)). In total, 372 PTCO/P die stacks and 15 tape frames were used in this experiment.
2. *Single-sided thermal-release tape sheet.*
   The white thermal-release tape has a thick polyester backing layer. Consequently, the tape is more solid than dicing tape and can be used as stand-alone carrier, i.e., without tape frame (see Figure 10(b)). Several tape sheets with PnP'd arrays of maximal 9×9=81 PTCO/P D2D stacks per sheet were produced and experimented with.



(a) Blue dicing tape on ⌀100mm tape frame. (b) Single-sided TR tape sheet. (c) Double-sided TR tape on ⌀300mm carrier wafer.

Figure 10: Three carriers with arrays of PnP'd PTCO/P D2D stacks.

3. *Double-sided thermal-release tape on carrier wafer.*
   The transparent double-sided thermal-release tape temporarily affixes die stacks on a blank ⌀300mm carrier wafer. This allow to automatically load the carrier wafers from wafer cassettes via the MHU load port. Several ⌀300mm carrier wafers with tape sheets with PnP'd arrays of maximal 7×7=49 PTCO/P D2D stacks per sheet were produced and experimented with (see Figure 10(c)).

3.3 Automatic Re-Align In Action

Figure 11 shows the automatic re-align procedure in action. Figure 11(a) shows a contact-view image, as seen through the side-view camera of the CM300 probe station [6]. At the top of the picture is the probe card, with the cantilever probe needles sticking out in the center down to the probe horizon [7]. The stacked PTCO dies can be seen in the bottom of the photo. In order to avoid that the probe card touches the stacked PTCO dies while probing on the probe pads located on the top side of the bottom PTCP die, we were using extra-long needle tips to compensate for the stacked-die height.

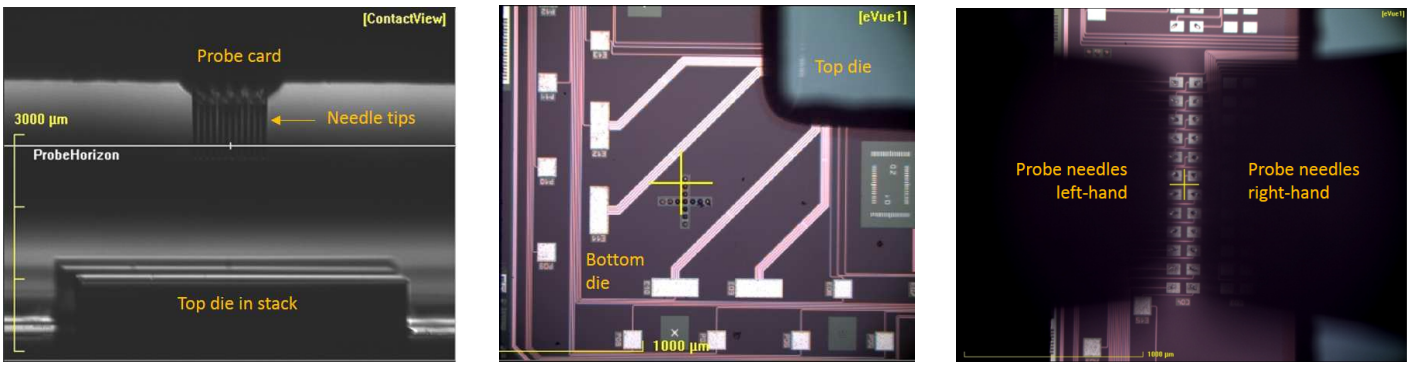
Figure 11(b) shows a detail photo of a bare D2D stack, taken by the top-view eVue1 camera of the prober. Most of the picture shows a part of the top side of the bottom die, with in the upper-left corner (in gray-blue) a partial view of the stacked top die. This picture was taken during the training of an alignment pattern; in this case, the alignment pattern was an alignment cross on the bottom die.

Figure 11(c) is again taken by the top-view eVue1 camera of the probe station. It shows the probe needles just after touching down on the 2×12 probe-pad module. The probe marks, nicely located in the center of the probe pads, validate the correct operation of the automatic re-align procedure.

4 Experimental Results

4.1 Results on Dicing Tape on Frame

The CM300 probe station is positioned in the clean-room area of IMEC's 300mm FAB2 and normally operated at 'Contamination Level 3' (= Cu contamination). The PnP'd tape frames are at Contamination Level 5. Consequently, we had to run the experiments with the tape frames for ⌀100mm wafers as a contamination exception, after which the probe station had to be cleaned to operate again at Contam Level 3. This cleaning procedure was effective, as proven by total reflection X-ray fluorescence (TXRF) witness wafers.



(a) Probe needles and die stacks; contact view from side-view camera. (b) Detail of the die stack; downward view from top-view camera. (c) Probe needles above pads; downward view from top-view camera.

Figure 11: The automatic re-align procedure on the CM300 probe station in action.

The tape frames for ⌀100mm wafers were loaded manually onto the chuck of the CM300 probe station via it's front-side manual load port. Some of the (reused) tape frames suffered from a slight bend (see Figure 12). Also, due to the manual lamination of the blue dicing tape onto the tape frames, some tapes suffered from several visible wrinkles (see Figure 13(a)). The bent frames and tape wrinkles caused some vacuum leakage at the probe station's chuck. In addition, it is impossible for the probe station to compensate for die stacks which are tilted due to tape wrinkles. Fortunately, most tape wrinkles disappeared after spending one night on the vacuum chuck and some manual 'ironing' with the engineer's fingers (see Figure 13(b)).

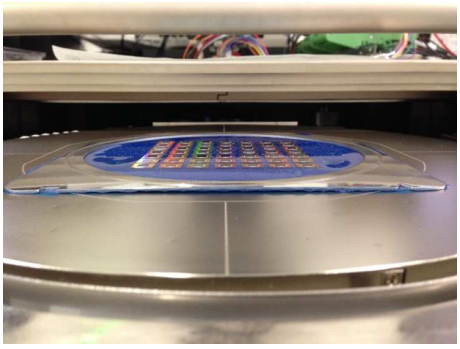
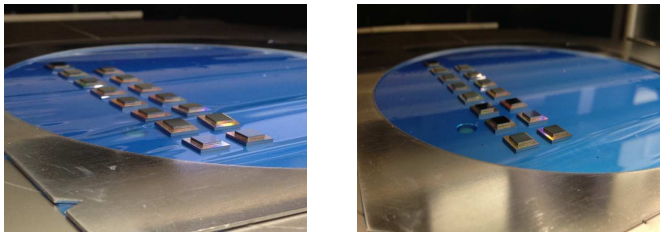


Figure 12: Used tape frame with slight bend.



(a) Visible tape wrinkles. (b) Wrinkles almost gone.

Figure 13: Visible tape wrinkles (a) and wrinkles almost disappeared after manual 'ironing out' (b).

The PnP job was relatively difficult, as the blue dicing tape has flex-and-stretch behavior and no alignment markers. Consequently, the PnP tool underperformed in placement accuracy compared to its specification on a solid underground and in the presence of alignment markers. Table 1 lists the incremental corrections Δx_c, Δy_c, and $\Delta\theta_c$ as measured on the CM300 probe station for a particular tape frame with (only) 14 die stacks. Stack 8 was the pre-trained alignment position (the so-called *'home die'*), whereas Stack 1 was the start position for the ('snaking-down') probing sequence.

The automatic re-align algorithm as described in Section 2 generally worked well. In total, execution of *'AlignChip'* took about 30 seconds per die stack, for two invocations (Steps 3.6 and 3.8) on two alignment patterns (bottom-left corner and top-right corner).

Die Stack	Wafer Map Location	Δx_c (μm)	Δy_c (μm)	$\Delta\theta_c$ (°)
1	(0,0)	-110	59	0.065
2	(1,0)	-203	28	-0.079
3	(1,-1)	-86	113	0.177
4	(0,-1)	1	267	0.198
5	(0,-2)	-37	55	-0.275
6	(1,-2)	-39	55	0.069
7	(1,-3)	-20	91	-0.028
8	(0,-3)	0	0	-0.155
9	(0,-4)	-4	91	0.138
10	(1,-4)	8	51	-0.091
11*	(1,-5)	–	–	–
12	(0,-5)	-127	245	0.371
13	(0,-6)	-111	184	-0.079
14	(1,-6)	133	6	-0.388
Minimum (excl. *)		-203	0	-0.388
Maximum (excl. *)		+133	+267	+0.371
Average(abs) (excl. *)		±68	±96	±0.163
Std.dev(abs) (excl. *)		±62	±82	±0.112

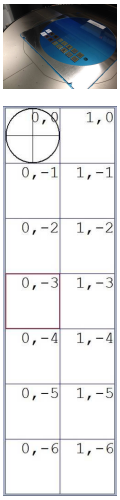
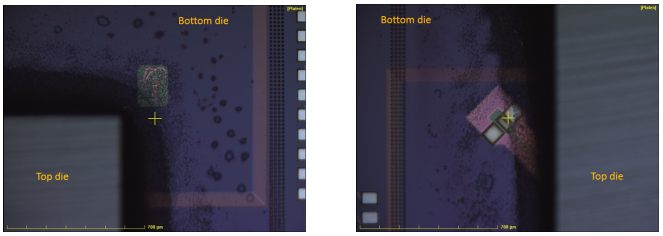


Table 1: Measured incremental PnP corrections on dicing tape.

We had only a few incidental cases where the re-align algorithm did not work properly (as was the case for Stack 11 on the tape frame described in Table 1).

- Two instances of die stacks were found to be 90° rotated. This was due to a manual mistake in preparing the die stacks for PnP operation. Obviously, the *'AlignChip'* procedure could not find the alignment patterns for these two cases.

- For two instances of die stacks, the alignment patterns were obscured by underfill fillet and underfill out-bleeding (see Figure 14). Note that the particular underfill material used in this case was a research path-finding material; the underfill supplier was aware of the issue and has improved it since. In this case, the fact that *'AlignChip'* can work with a second (back-up) alignment pattern might provide a solution, provided that the alternative alignment pattern is not obscured as well.



(a) Underfill fillet. (b) Underfill out-bleeding.

Figure 14: Underfill obscuring alignment patterns used for 'AlignChip'.

At the bottom of Table 1, the overall minimum, maximum, average, and standard deviation values are listed for all $14 - 1 = 13$ die stacks (excluding the anomalous Stack 11, marked with *).

4.2 Results on Single-Sided TR Tape

The tape sheets were loaded manually onto the chuck of the CM300 probe station via it's front-side manual load port (see Figure 15).

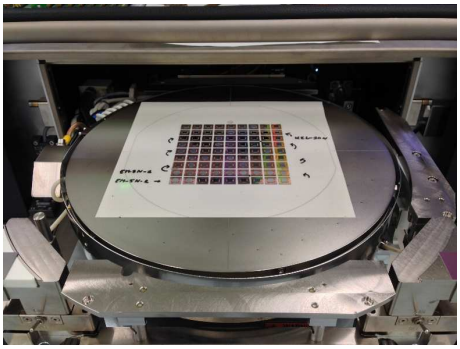
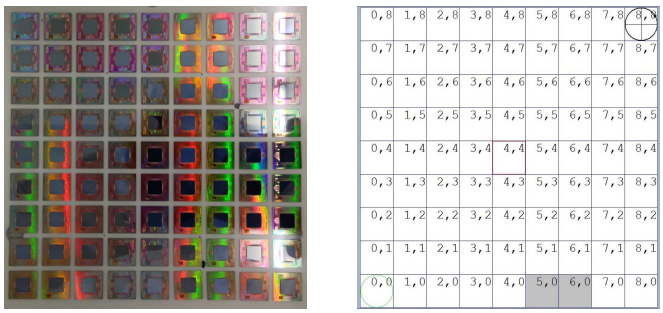


Figure 15: Loading a tape sheet with PnP'd die stacks onto the CM300's chuck via the prober's front-side manual load port.

Figure 16 shows a top-view photo and corresponding wafer map of an array of 9×9=81 PnP'd PTCO/P stacks on single-sided thermal-release tape. The center Stack 41 (= location (4,4)) was used as *'home die'*. The probing sequence started at Stack 1 (= location (0,0)) and 'snaked-up' to Stack 81 (= location (8,8)).



(a) Top-view photo. (b) Wafer map.

Figure 16: Array of 9×9=81 PnP'd PTCO/P stacks on single-sided TR tape.

Again, the automatic re-align algorithm as described in Section 2 generally worked well. In order to save execution time, we decided to skip the second invocation of *'AlignChip'* (Step 3.8). Table 2 lists the incremental corrections Δx_c, Δy_c, and $\Delta\theta_c$ as identified by the CM300 prober for all 81 die stacks, as well as the time t_{AC} (in seconds) it took *'AlignChip'* to correct the misalignment and the time t_{SND} (in seconds) used by *'StepNextDie'* to jump to the next die stack.

As can be seen in Table 2, there were some incidental problems with *'AlignChip'*, due to an exceptionally large stack rotation angle θ_c.

- Stacks 6 and 7 had a rotation angle θ_c too large for *'AlignChip'*. The workaround was to exclude them from the wafer map (see grayed out positions in the wafer map in Figure 16(b)), such that the probe station would skip them and jump from Stack 5 immediately to Stack 8.
- Stack 45 had a large rotation angle θ_c; not too large for *'AlignChip'* too handle, but large enough for the probe station too lose its way after jumping to the next stacks. The prober spent around 47 unsuccessful seconds on *'AlignChip'* for both Stacks 46 and 47, in order to get itself on track again from Stack 48 onwards.

At the bottom of Table 2, the overall minimum, maximum, average, and standard deviation values are listed for all $81 - 6 = 75$ die stacks (excluding the anomalous die stacks, marked with *). Note that the misalignments on the single-sided thermal-release tape are significantly smaller than on blue dicing tape (using the same die stacks and the same PnP machine); consequently the average *'AlignChip'* execution time was reduced.

The thermal-release tape has a thick polyester backing layer. The tape is more solid than dicing tape and can be used as stand-alone carrier. Consequently, the sheets of thermal-release tape provide various benefits over the dicing tape on tape frames.

- No need for tape frames, and hence no risk of bent tape frames.
- No tape wrinkling.
- Less flex-n-stretch behavior, due to which the resulting placement of the PnP tool becomes much better. Consequently:
  - The 'street' spacing between PnP'd die stacks could be minimized, such that we could accommodate larger arrays of die stacks and hence maximize the test throughput;
  - The *'AlignChip'* execution time went down from ∼15 seconds to on average 13.1 seconds per die stack.

4.3 Results on Double-Sided TR Tape

The ⌀300mm blank carrier wafers with a sheet with PnP'd die stacks were loaded automatically onto the chuck of the CM300 probe station from a front opening unified pod (FOUP) wafer cassette at the MHU load port. Figure 17 shows a photo of such a populated carrier wafer inside the MHU.

Figure 18 shows the 'wafer' map of an array of $7 \times 6 - 7 = 35$ PnP'd PTCO/P stacks on a sheet of double-sided thermal-release tape on a ⌀300mm carrier wafer. Note that the grayed-out locations were not populated with die stacks in this particular array. In order to reduce execution time, we unified the *'home die'* and the *'start die'*, in this case both Stack 1 (= location (0,0)).

Die Stack	Wafer Map Location	Δx_c (μm)	Δy_c (μm)	$\Delta\theta_c$ (°)	t_{AC} (s)	t_{SND} (s)
1	(0,0)	-6.5	-57.0	-0.083	13.3	0.9
2	(1,0)	-66.0	11.0	0.073	14.0	0.9
3	(2,0)	-15.2	-9.4	-0.070	14.2	1.0
4	(3,0)	-12.4	-11.2	-0.051	12.9	1.0
5	(4,0)	-20.0	8.1	-0.001	13.0	1.5
6*	(5,0)	–	–	–	–	–
7*	(6,0)	–	–	–	–	–
8	(7,0)	49.9	39.3	0.030	13.0	1.0
9	(8,0)	46.5	49.7	0.045	13.1	0.9
10	(8,1)	29.5	47.2	0.030	12.9	0.9
11	(7,1)	34.1	35.5	0.095	12.8	0.9
12	(6,1)	42.1	25.1	0.035	13.1	0.9
13	(5,1)	47.3	20.3	0.091	13.2	1.0
14	(4,1)	53.4	5.9	-0.002	12.9	0.9
15	(3,1)	57.8	-12.5	0.019	12.9	0.9
16	(2,1)	63.4	-28.5	0.039	12.9	0.8
17	(1,1)	69.9	-40.7	-0.029	13.1	1.0
18	(0,1)	3.7	58.2	0.120	14.2	0.9
19	(0,2)	13.5	49.0	-0.042	12.8	0.9
20	(1,2)	56.3	-42.7	-0.131	14.0	0.9
21	(2,2)	52.1	-27.9	-0.003	13.1	0.9
22	(3,2)	48.0	-15.9	0.041	13.0	1.0
23	(4,2)	38.4	0.7	0.070	13.1	0.9
24	(5,2)	34.5	15.9	0.052	13.1	0.9
25	(6,2)	28.3	25.6	0.012	13.0	0.9
26	(7,2)	46.2	77.7	-0.061	14.3	0.9
27	(8,2)	9.3	31.6	0.071	14.0	0.9
28	(8,3)	-21.9	-36.6	0.080	14.3	0.9
29	(7,3)	5.5	29.2	-0.094	14.1	0.9
30	(6,3)	9.3	18.4	0.029	13.0	0.9
31	(5,3)	15.6	12.7	0.056	13.1	0.9
32	(4,3)	17.0	1.4	0.094	12.9	0.9
33	(3,3)	21.4	-15.0	0.092	13.0	0.9
34	(2,3)	31.2	-22.3	-0.005	13.0	0.9
35	(1,3)	36.3	-37.1	-0.005	13.1	0.8
36	(0,3)	41.5	-44.7	0.077	12.7	1.0
37	(0,4)	29.3	-47.5	0.024	12.8	1.0
38	(1,4)	23.5	-37.5	0.054	13.1	1.0
39	(2,4)	15.5	-27.0	0.029	12.7	1.0
40	(3,4)	11.0	-13.6	0.025	13.0	1.0
41	(4,4)	7.4	-5.8	-0.028	12.7	1.0
42	(5,4)	1.8	6.4	-0.090	13.0	1.0
43	(6,4)	-0.1	24.2	0.080	13.1	1.0
44	(7,4)	-4.9	47.6	0.093	12.7	1.0
45*	(8,4)	-105.2	1399.3	-1.771	15.3	1.0
46*	(8,5)	–	–	–	47.1	0.8
47*	(7,5)	–	–	–	47.2	0.8
48*	(6,5)	-22.3	24.9	1.748	20.9	0.9
49	(5,5)	-14.8	8.4	0.004	12.7	0.9
50	(4,5)	-13.4	-17.0	-0.085	12.7	0.9
51	(3,5)	-16.2	-14.6	-0.064	13.9	0.9
52	(2,5)	2.1	-30.6	0.074	14.0	0.9
53	(1,5)	16.1	-33.4	0.066	12.7	0.8
54	(0,5)	14.9	-57.0	0.055	12.7	1.0
55	(0,6)	70.1	65.1	0.137	13.9	0.9
56	(1,6)	63.3	48.9	-0.075	12.7	0.9
57	(2,6)	3.2	-17.6	-0.116	13.9	0.9
58	(3,6)	-0.8	-15.2	-0.040	13.1	1.0
59	(4,6)	-6.2	-5.0	-0.026	13.0	1.0
60	(5,6)	-15.8	-3.0	-0.003	13.1	0.9
61	(6,6)	-20.6	-1.6	-0.055	12.6	0.9
62	(7,6)	-25.6	6.3	-0.002	13.0	0.9
63	(8,6)	-31.4	14.5	0.001	12.7	1.0
64	(8,7)	-36.6	10.5	-0.072	12.7	0.9
65	(7,7)	-32.0	5.9	-0.046	12.7	0.9
66	(6,7)	-28.0	0.5	-0.012	12.7	0.9
67	(5,7)	-23.0	-7.0	0.003	13.0	0.9
68	(4,7)	-16.6	-8.6	0.022	12.7	0.9
69	(3,7)	-8.8	-20.0	-0.005	12.8	0.9
70	(2,7)	-4.0	-22.0	0.065	13.1	0.9
71	(1,7)	2.5	-32.6	0.001	12.9	0.9
72	(0,7)	9.3	-40.6	-0.014	13.0	0.8
73	(0,8)	1.3	-42.2	-0.024	12.8	1.0
74	(1,8)	-6.1	-35.8	0.003	12.7	0.9
75	(2,8)	-11.3	-25.8	0.006	12.9	0.9
76	(3,8)	-15.5	-21.6	-0.029	13.0	0.9
77	(4,8)	-23.8	-17.0	-0.038	13.1	1.0
78	(5,8)	-30.6	-8.1	0.005	13.0	1.0
79	(6,8)	-34.2	-2.1	-0.013	12.7	1.0
80	(7,8)	-40.2	3.1	-0.053	12.7	1.0
81	(8,8)	-50.6	8.5	0.045	12.9	–
Minimum (excl. *)		-66.0	-57.0	-0.131	12.6	0.8
Maximum (excl. *)		+70.1	+77.7	+0.137	14.3	1.5
Average(abs) (excl. *)		±25.7	±24.3	±0.047	13.1	0.9
Std.dev(abs) (excl. *)		±18.9	±17.6	±0.035	0.5	0.1

Table 2: Measured incremental PnP corrections and execution times on single-sided thermal-release tape.

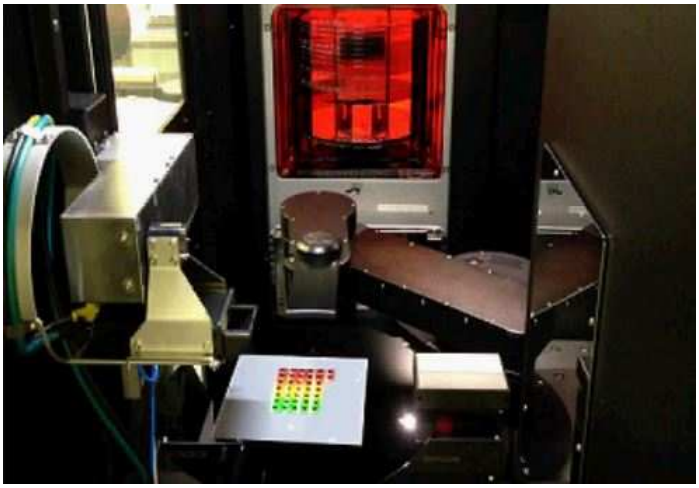


Figure 17: Carrier wafer with a sheet with PnP'd die stacks in the MHU.

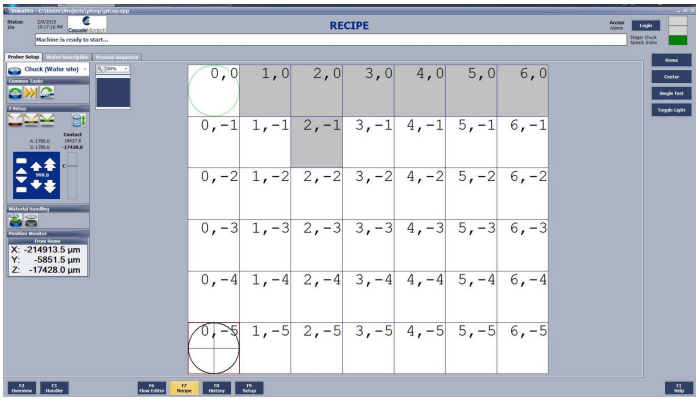


Figure 18: Wafer map of an array of 7×6-7=35 PnP'd PTCO/P stacks on double-sided thermal-release tape.

Die Stack	Wafer Map Location	Δx_c (μm)	Δy_c (μm)	$\Delta\theta_c$ (°)	t_{AC} (s)	t_{SND} (s)
1	(0,0)	-0.2	-0.2	-0.004	5.4	2.1
2	(6,-1)	21.3	47.2	-0.035	5.6	1.1
3	(5,-1)	21.3	61.1	-0.035	5.5	0.8
4	(4,-1)	17.0	70.0	-0.045	5.6	0.9
5	(3,-1)	12.4	74.9	0.013	5.5	1.1
6	(1,-1)	-16.1	66.4	-0.062	6.5	0.9
7	(0,-1)	19.3	64.2	0.048	5.5	1.0
8	(0,-2)	-10.0	160.1	0.040	5.5	0.9
9	(1,-2)	-5.7	160.0	0.014	5.5	0.9
10	(2,-2)	-8.8	162.7	0.012	5.5	0.8
11	(3,-2)	-4.6	167.2	-0.003	5.5	0.9
12	(4,-2)	2.9	176.2	0.036	5.7	0.9
13	(5,-2)	-1.3	177.0	0.039	5.5	0.9
14	(6,-2)	6.4	180.3	0.019	5.6	0.9
15	(6,-3)	10.4	293.2	0.060	6.7	0.8
16	(5,-3)	8.6	297.2	-0.042	5.4	0.8
17	(4,-3)	8.8	313.8	0.004	5.6	0.9
18	(3,-3)	4.6	312.3	0.022	5.4	0.8
19	(2,-3)	-0.6	310.4	-0.012	5.5	0.9
20	(1,-3)	-3.3	319.2	-0.020	5.6	0.8
21	(0,-3)	-5.5	286.4	-0.045	5.5	0.9
22	(0,-4)	-8.2	330.0	-0.043	5.5	0.9
23	(1,-4)	9.2	293.2	-0.072	6.7	0.9
24	(2,-4)	0.7	302.1	0.062	6.7	0.9
25	(3,-4)	3.2	298.1	0.014	5.5	0.8
26	(4,-4)	3.3	282.9	-0.016	5.4	0.9
27	(5,-4)	28.3	305.2	-0.064	6.7	0.8
28	(6,-4)	-0.3	229.6	0.113	6.8	0.9
29	(6,-5)	18.8	369.5	-0.071	6.8	0.9
30	(5,-5)	11.4	373.8	-0.029	5.5	0.9
31	(4,-5)	8.6	389.0	0.045	5.6	0.9
32	(3,-5)	7.0	387.8	-0.028	5.6	0.8
33	(2,-5)	-2.3	397.4	0.027	5.4	0.9
34	(1,-5)	23.6	386.3	-0.055	12.1	0.8
35	(0,-5)	16.9	378.5	0.002	5.5	–
Minimum		-19.3	-0.2	-0.072	5.4	0.8
Maximum		+28.3	+397.4	+0.113	12.1	2.1
Average(abs)		±9.5	±240.7	±0.036	5.9	0.9
Std.dev(abs)		±7.3	±116.9	±0.024	1.2	0.2

Table 3: Measured incremental PnP corrections and execution times on double-sided thermal-release tape.

Again, the automatic re-align algorithm as described in Section 2 worked well. Table 3 lists the incremental corrections Δx_c, Δy_c, and $\Delta\theta_c$ as identified by the CM300 prober for all 35 die stacks, as well as the time t_{AC} (in seconds) it took *'AlignChip'* to correct the misalignment and the time t_{SND} (in seconds) used by *'StepNextDie'* to jump to the next die stack.

In order to save execution time, we decided to train *'AlignChip'* only on one alignment pattern and skip the second invocation of *'AlignChip'* (Step 3.8) altogether. This brought down the average time spent on *'AlignChip'* to 5.9 seconds. Note that this is still longer than the time t_{SND} required for stepping to the next die (0.9 seconds), but significantly smaller than manual alignment.

5 Tape Frames for ⌀300mm Wafers

Figure 19 shows the specification of the SEMI standard G74-0669 for tape frames for wafers of ⌀300mm [8]. The tape frame is necessarily larger than the ⌀300mm wafer it holds; the inner diameter (A) is 350mm, the outer diameter (B) is 400mm, and the width (C) and height (D) are 380mm.

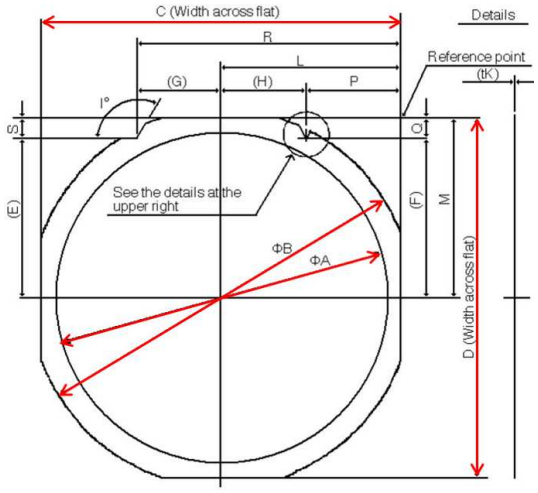


Figure 19: Specification of SEMI G74-0669 tape frame for ⌀300mm wafers (source: SEMI, [8]).

Today's state-of-the-art probe stations handle wafers up to ⌀300mm. The CM300 probe station has been extended to be able to handle these larger tape frames in semi-automatic mode, i.e., with manual loading through the front-side load port. From the start of the architectural design of this new prober type, extra maneuver space was foreseen, such that the large tape frames can be moved around by the chuck without hitting things. The probe station's upward-looking chuck camera (required for support of vertical, non-see-through, probe cards) was repositioned, such that the tape frame does not block the view of the chuck camera. Finally, mechanical supports were added to the chuck system for carrying the weight of the metal tape frame. These supports were designed such that they leave probe access to auxiliary chucks (used for calibration and probe tip cleaning substrates), provide alignment guidance to the operator, and can be used in either a left-hand or right-hand prober version. A CAD view of the final design is depicted in Figure 20.

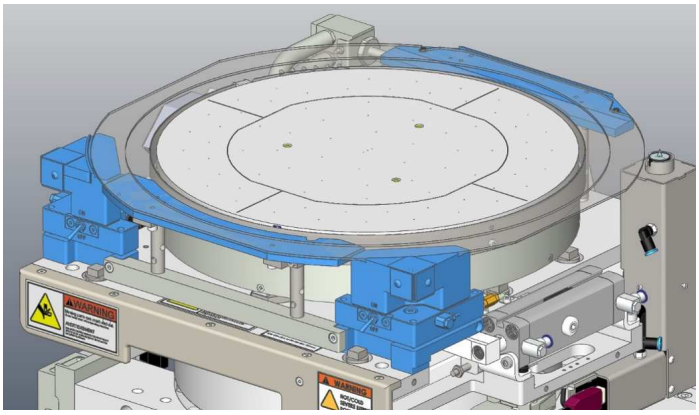


Figure 20: CM300 tape-frame support for SEMI G74-0669 [8].

This tape-frame support is installed and tested at IMEC. Use scenarios in the context of testing 3D-SICs are (1) as carrier for PnP'd bare die stacks in order to enable automatic index-step probing (as reported in this paper), and (2) probing on ⌀300mm wafers that are thinned down in order to expose their through-silicon vias (TSVs), for which the tape frame serves as a temporary carrier.

6 Conclusion

In this paper, we have demonstrated the feasibility of automatically probing and index-stepping over an array of PnP'd bare D2D stacks on a carrier substrate. We described an algorithm based on the *'AlignChip'* function of Cascade Microtech's CM300 probe station to automatically correct small PnP misalignments. We presented experimental results for three types of carriers: (1) dicing tape on tape frames for ⌀100mm wafers, (2) sheets of single-sided thermal-release tape, and (3) ⌀300mm carrier wafers with double-sided thermal-release tape. Misalignment correction was equally successful on all three types of carriers. Its success is due to the large FoV of the CM300's platen camera, but critically depends on rotational misalignments remaining sufficiently small and the alignment patterns not being obscured. For the latter situation, *'AlignChip'* can work with a second (back-up) alignment pattern. However, in most cases one pattern suffices, taking on average less than 6 seconds alignment time per die stack. This constitutes a significant improvement over manual alignment of individual bare D2D stacks and allows automated, unattended testing of PnP'd arrays of stacks.

Our tape frames were sometimes bent and the manually laminated dicing tape on them sometimes showed wrinkles, causing issues with the chuck's vacuum operation; those problems were absent for the thermal-release tapes. Carrier wafers with double-sided thermal-release tape have as additional benefit that they enable usage of the probe station's auto-loader.

Finally we described a recent extension to the CM300 probe station, enabling manual loading of 400mm-wide tape frames for ⌀300mm wafers.

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