Improving Signal Fidelity in High Parallelism Probe Card via TTRE

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Introduction

Focus of this discussion

- ## What this paper is "not"
    - SI/PI probe card design
    - FFI TRE
    - FFI ATRE and ATRE control method

- ## What this paper will discuss -
    - Using FFI Terminated TRE (**TTRE**) to achieve improved signal fidelity and enable higher signal sharing while maintaining or increasing test speed

TTRE is FFI patent protected

Outline

- **Introduction of Terminated TRE (TTRE)**
  - Signal line termination
  - DUT parallelism trend
- **TTRE overcoming challenges of tester resource sharing**
  - Signal degradation with higher TRE-share
  - Limitation on the number of signals shared
- **Case study review**
- **Summary / Conclusion**
- **Follow-on work**

Introduction

Increasing probe card parallelism with Advanced TRE

- **Probe card DUT parallelism is trending higher enabled by higher signal sharing**

- **ATRE – Advanced tester resource enhancement/extension**

  - DC and Power (PPS-TRE) with active components

- **TRE / TTRE – DC signal share**

  - TRE: signal and driver sharing without active components

  - Terminated TRE (TTRE): driver sharing with active components

- **TTRE – recommended for TRE share of x14 or higher to improve signal performance and to increase test speed to 200MHz**

- **Address 1X, 1Y, 1Z process node transition**

TTRE is FFI patent protected

Signal TRE and TTRE

≤ 200MHz
TTRE not required

1Z

1Y   x16-x32

x14-x22

1X

x8-x12

≤ x8

TTRE enables 200MHz with improved signal

Probe Card Parallelism: 3520, 2112, 1536, 768, 512

T5377 MT6050 | T5383 MT6121 | T5385 Magnum MT6123 | T5386/T5833 Magnum MT6133 | NGT ATEs
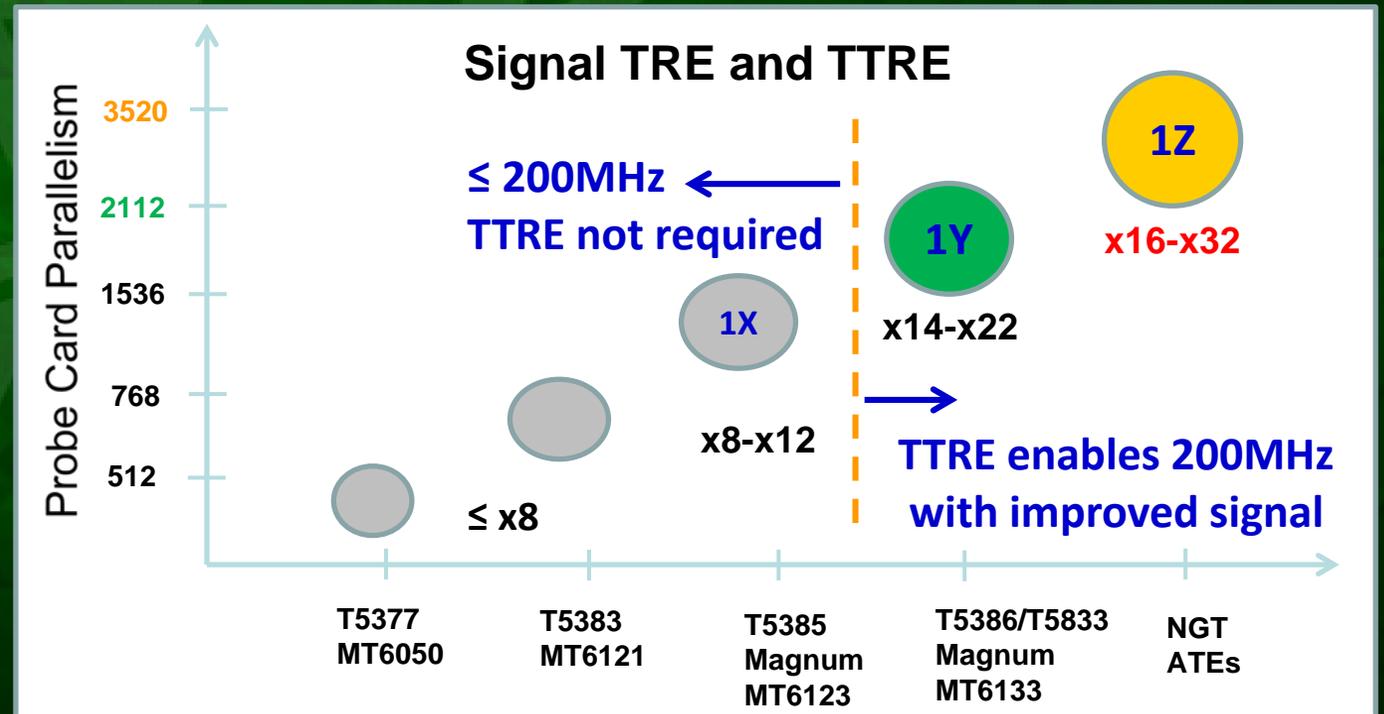
Introduction

What are TRE, ATRE, and TTRE ?

Introduction

- **Test Resource Enhancement = TRE**
  – Sharing of tester resources between multiple DUTs using passive components.

- **Advanced TRE**
  – Sharing of test resources using active components and having the ability to connect and disconnect DUTs from the tester resources

  – Other active circuits to increase tester capabilities
    • Current, Frequency …

Michael Huebner

June 9 - 12, 2013
IEEE Workshop

3

And the new TTRE
= Terminated-TRE

TTRE technology improves signal condition which allows

(1) Increased/doubled test speed without compromising signal integrity

(2) Increased signal sharing without compromising test speed

TTRE is FFI patent protected

Signal Fidelity Impacted by Higher Sharing
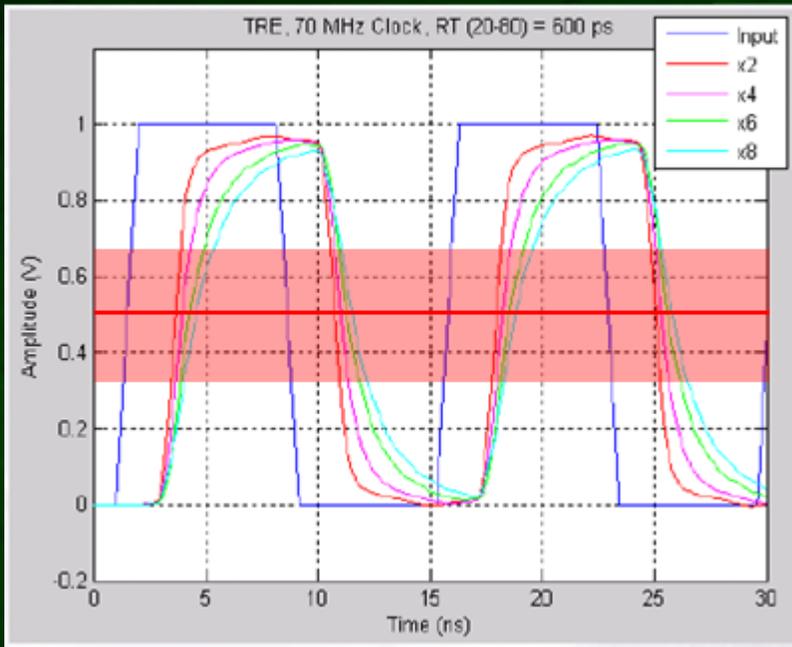
- **Key signal integrity considerations**
  - Slow down rise time
  - Reduce signal amplitude
  - Increases signal skew

- **Potential contribution to data-eye shrinkage**
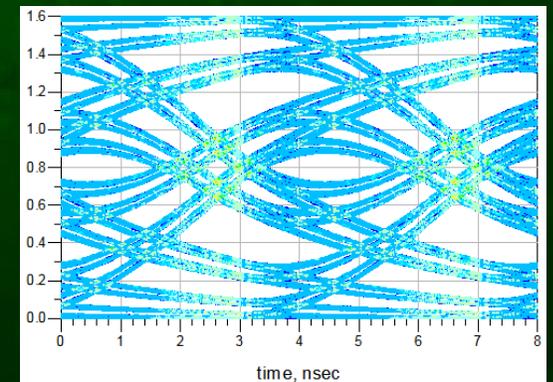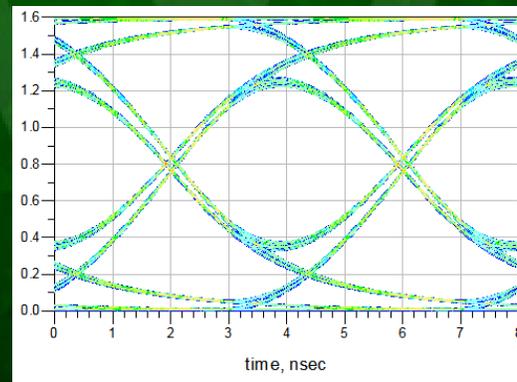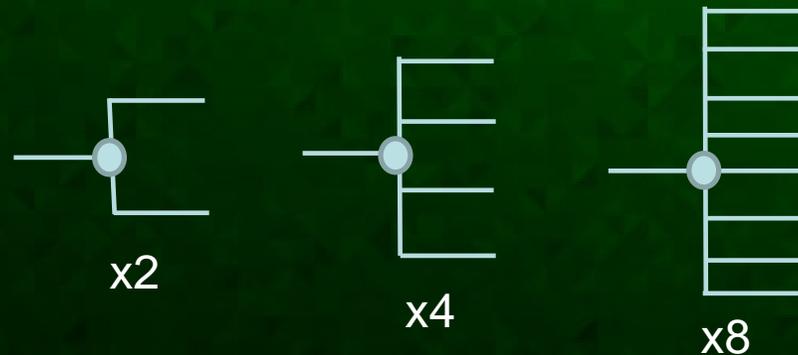
**Example of signal impacted by sharing factor**

x2

x4

x8

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Signal Fidelity Improves with Termination

- **Typical Issues with Signal Sharing/Splitting**
  - **Voltage reflection at PCB to Share points**
  - **These cause driver signal arbitrations that limit performance**
    - **Amplitude, rise time, etc.**

- **TTRE absorbed the reflections, enhanced the signal**
  - **Minimized signal reflections from V-share back to driver**
  - **Absorb reflection from VDUT back to V-share and source**
  - **Significant improvement in waveform at the DUT**
    - **Increase amplitude, restore rise time**

Implementing FFI TTRE – Terminated TRE
Advanced circuitry with active component and termination power supply
FFI design and fabricated TTRE module with density to support 1TD
~3000 DUT parallelism
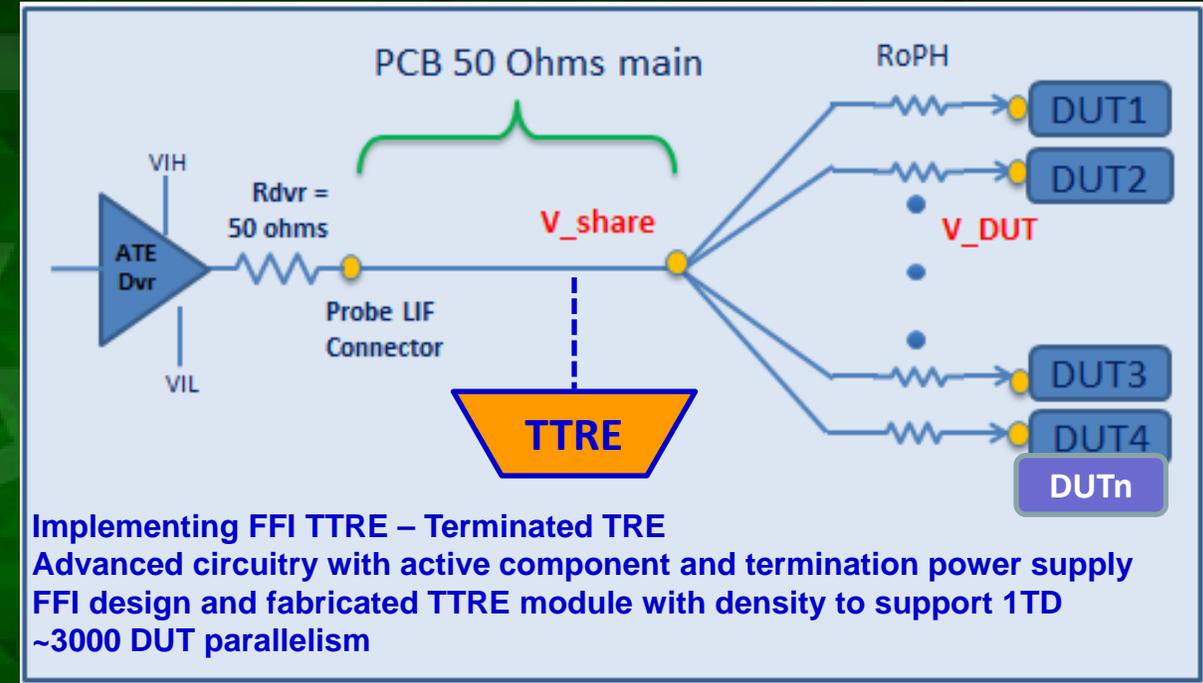
TTRE is FFI patent protected
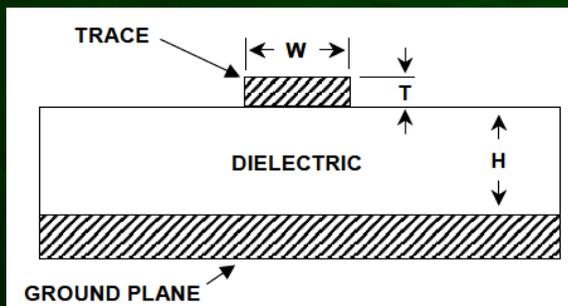
Characteristic Impedance fundamentals

$$Z_O(\Omega) = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left[\frac{5.98H}{(0.8W + T)}\right]$$

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Key Benefits of TTRE Implementation

- **Enables higher parallelism (>1536DUT) while maintaining test speed at ≤125MHz**
  - Without TTRE higher signal sharing reduces signal fidelity
    - Slower rise time, reduction of amplitude
- **Maintaining parallelism (1536DUT or 2112DUT) while increasing test speed from 100MHz to 200MHz**
  - Better signal fidelity at higher test frequency
- **Improve throughput and test efficiency**
  - Test coverage increases with test frequency increases
- **Extend life time and ROI on existing tester fleet**
- **Package device to wafer sort test result correlation at elevated 200MHz**

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TTRE Implementation Considerations

There are different ways to implement TTRE depending on tester capability

- Termination values (RT and VTT) selected according to signal performance, power dissipation, and tester driver capability
  - (i.e. 28ohm, 45ohm, or 57ohm based on # of share)

- Internal switch available to isolate TTRE during DC and low speed testing

- TTRE power supply provided on probe card
  - Programmable from ATE voltage resource (e.g. un used driver, DC channel or PPS)

Typical Tester Channel with TTRE Implementation

- **Address / command clocks and differential inputs**
  - CS_A
  - DQ_A
  - CK_T_A
  - CK_C_A
  - DQS_T_A
  - DQS_C_A
  - CA & WCK (for DDR5/LPDDR5)

- **Typical test items improve with higher test frequency**
  - Easy functional
  - Complex functional

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Case Study: >10-TRE Share Analysis

- ## Simulation conditions

  – Frequency = 100MHz, 175MHz and 200MHz

  – Vin = 1.1V, VTT = Vin/2

  – Magnum5 Tester

  – 1.0pF Load

| ATE driver input tR, input voltage | → | Probe Card VNA Measured S-parameter | → | DUT 1pF cap load |

- Keysight ADS
- Cadence Sigrity

Data eye evaluation point

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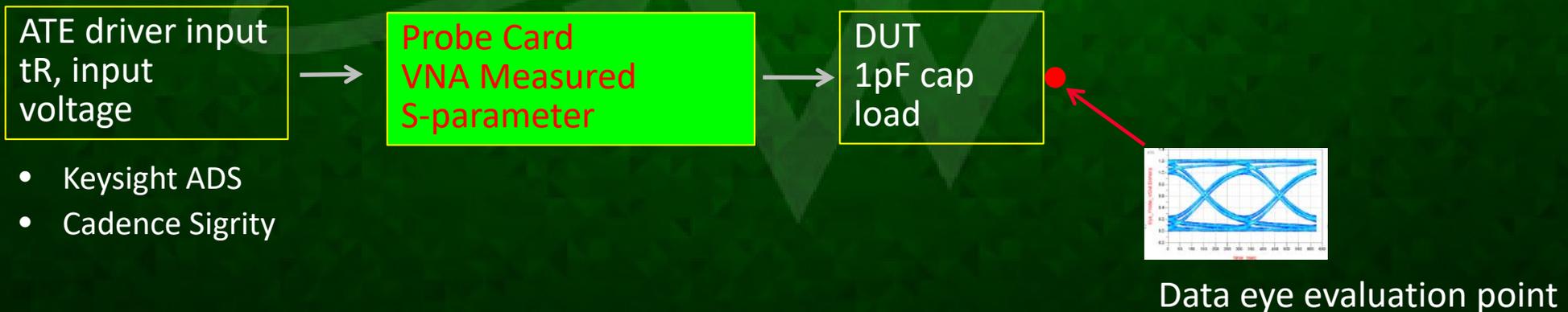
>10-TRE Share, 1.1V, 100MHz, 175MHz, 200MHz

Without TTRE

With TTRE

100Mhz

175Mhz

200Mhz

FFI TTRE

Enables
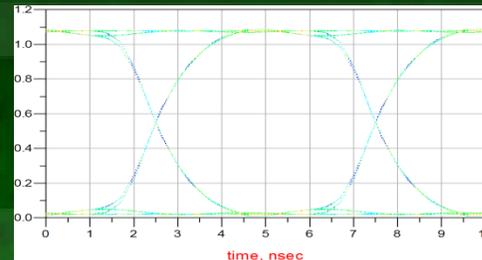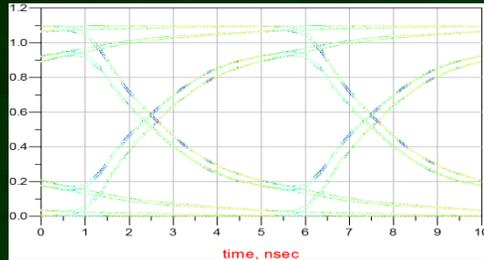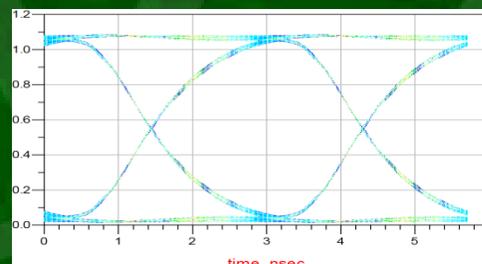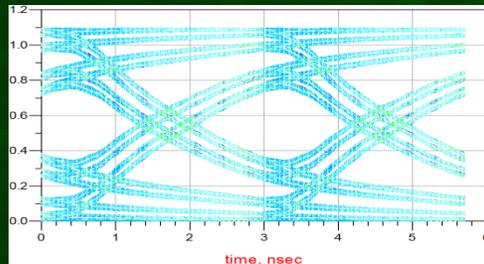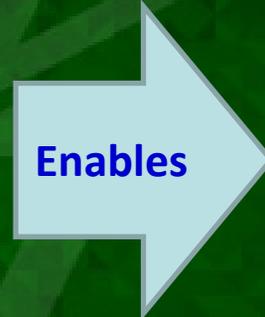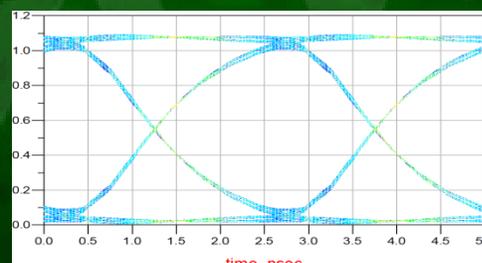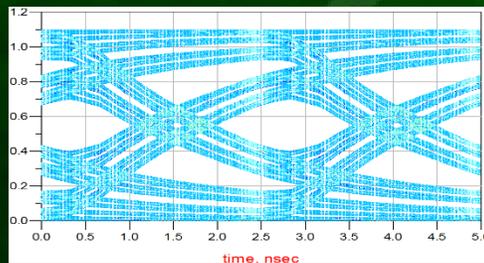
- ✓ **Higher ATE signal resource sharing while maintaining test quality**

- ✓ **Higher probe card parallelism for 1TD i.e. 2000 to 3000DUT**

- ✓ **Double speed from 100MHz to 200MHz without compromising test quality**

- ✓ **Early time to PGK test result at 200MHz**

- **TTRE greatly improves signal amplitude and overall data-eye opening**

Case Study Review

- ## X16-TRE Design with TTRE for LPDDR4

Parameter	ML9431A
Device	LPDDR4
Tester	MGV 24 Site
# of TTRE Module	~200
Max Parallelism Supported	1536 2048 (16SA)
Probe count	>100K
Touchdown	1TD
Total net count	~25K
Total switch count	
DC & PPS TRE IC	~200 XDC Boost

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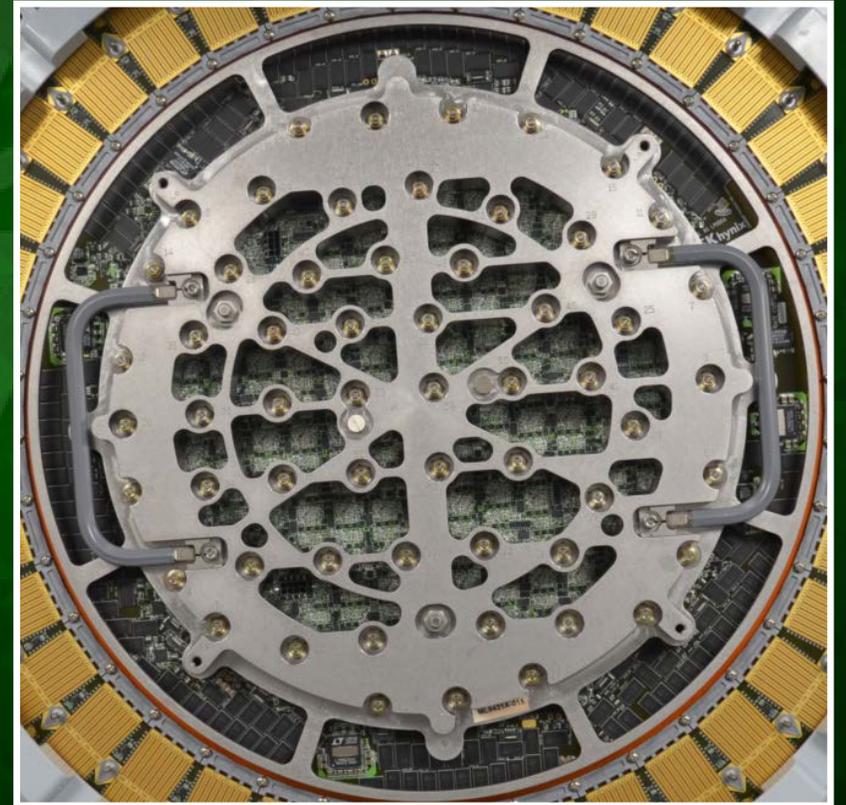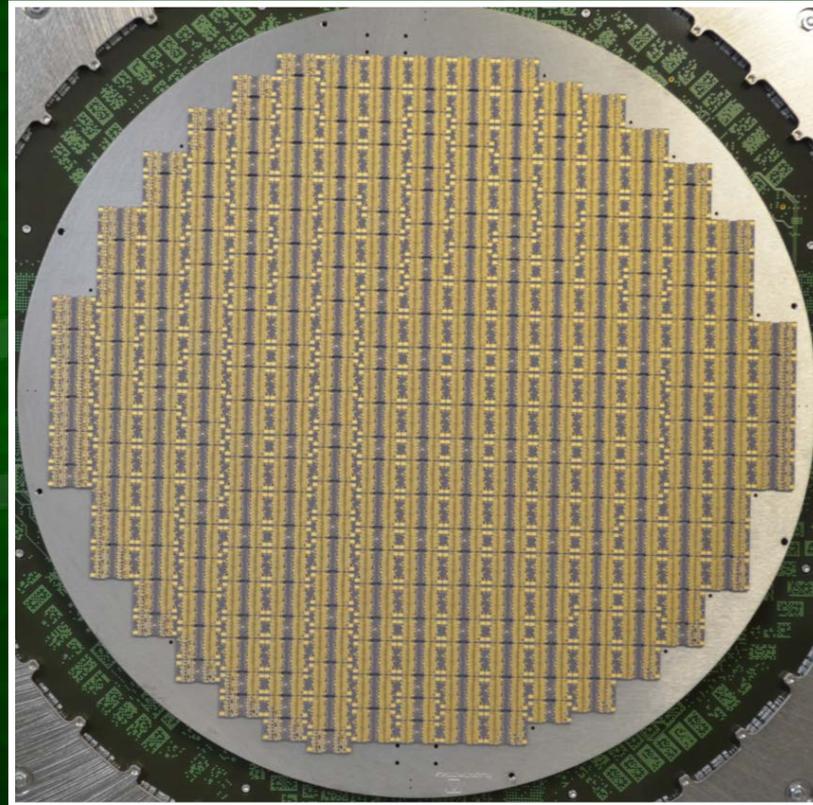
Actual Wafer Test Measurement

- **Overall efficiency achieved depends on the number of frequency related test items implemented and test strategy**

- **Proven test frequency doubled from 100Mhz to 200Mhz in production environment for DDR4/LPDDR4 type memory (1X and 1Y node)**
  - Correlated between wafer test and final package test result

  - No deviation from fail bit count

ATE Test Program Considerations

- **Test Program considerations for TTRE Implementation**

  - PPS channel assignment of dummy DUT to set up the reference level.

  - Tester spec consideration for TTRE power consumption.

  - Control bit assignment for TTRE On/Off.

  - VIH/VIL level adjustment by each test items.

    --> Consider levels based on VIH / VIL variables

	VTT = 0.75V setting @ 1.5V Operation			
ATE VIH	1.5V	2.0V	**2.8V**	3.5V
DUT VIH	1.03V	1.22V	**1.52V**	1.78V
ATE VIL	0V	-0.5V	**-1.25V**	-1.25V
DUT VIL	0.47V	0.28V	**0.00V**	0.0V

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Device Specific Test Correlation

- **Device specifics test results**

  - **Performance improvement in term of test speed**
    - ① Successfully achieved test speed increased from 100Mhz to 200Mhz
    - ② Function test time reduction

  - **Strong 100Mhz Vs. 200Mhz wafer test correlation results**
    - ① No deviation from wafer fail bit count

  - **Strong Wafer test Vs. PKG test correlation results**
    - ① No deviation from fail rate & yield

100MHz to 200MHz Correlation
200Mhz / 100Mhz
[Wafer fail bit count]

PKG Test to Wafer Test Correlation
PKG Test / Wafer Test
[fail Rate]
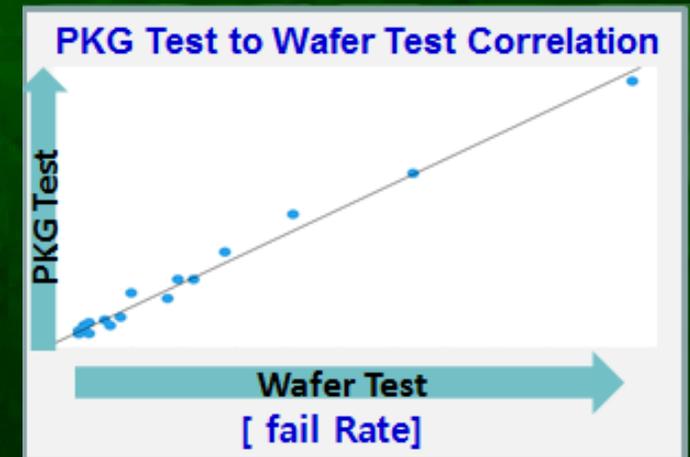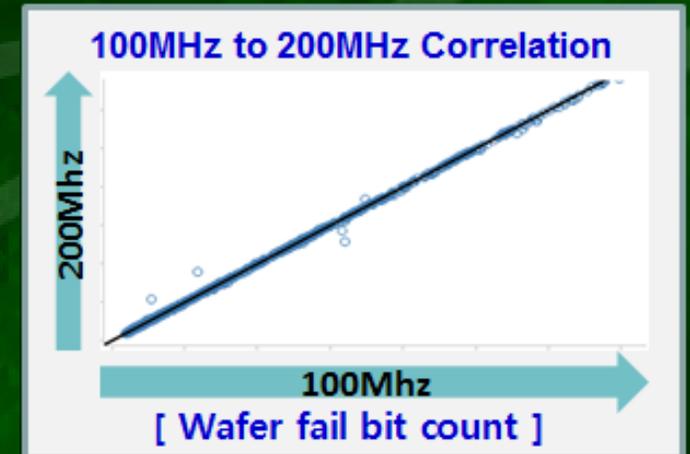
Summary / Conclusion

- **Terminated TRE (TTRE) significantly improves signal fidelity, enables higher tester resource sharing as DRAM node transitions to 1X, 1Y, and 1Z on existing testers**
  - Higher test frequency with wider and larger data-eye
  - Higher probe card DUT parallelism
- **By doubling test frequency from 100MHz to 200MHz, TTRE improves test throughput and efficiency**
  - Faster clock, more efficient functional tests
- **Enable correlation and early time to data for packaged test result at 200MHz**
 - No deviation from wafer test & package test result at elevated test speed of 200MHz

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Follow-on Work

- **Implementing and validating TTRE at TRE-share >x30 to enable 1TD testing of ~2500 and ~3000DPW using existing ATE**

  – Enabling testing of DRAM 1Z process node transition

  – 1TD, 200K probes per probe card, ~3000DUT parallelism

- **Data-eye opening performance improvement with FFI TTRE technology**

  o **No TTRE**
  o **>x30-TRE Share**
  o **125Mhz**

  o **With FFI TTRE**
  o **>x30-TRE Share**
  o **125Mhz**

FFI TTRE

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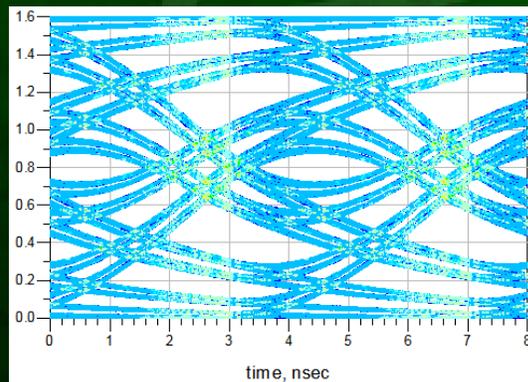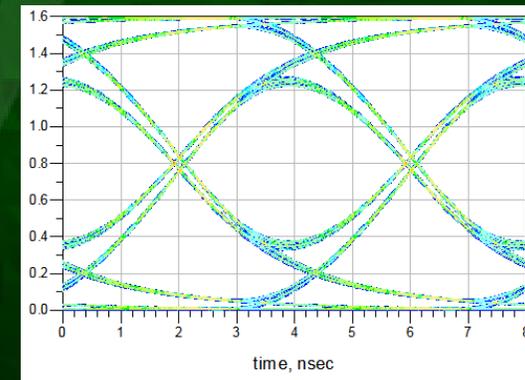
Thank You - Questions

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