Enabling Vertical Super High Probe Counts at Wafer Test

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Agenda

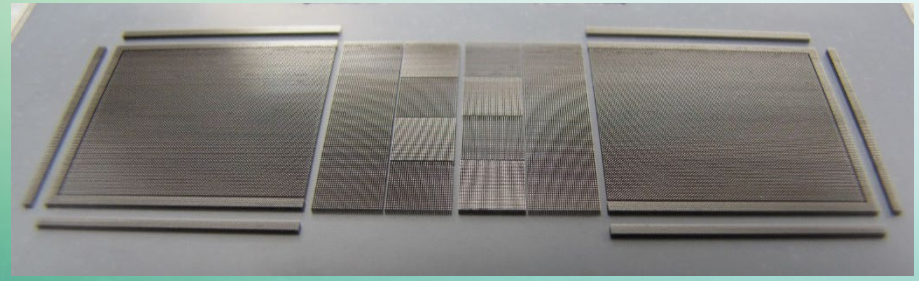
- Probe count trends
- Understanding actual overtravel
- Impact of system stiffness
- Thermal effects
- Guide plate and MLO challenges
- Equipment readiness
- Conclusions

Why Is Probe Count Increasing?

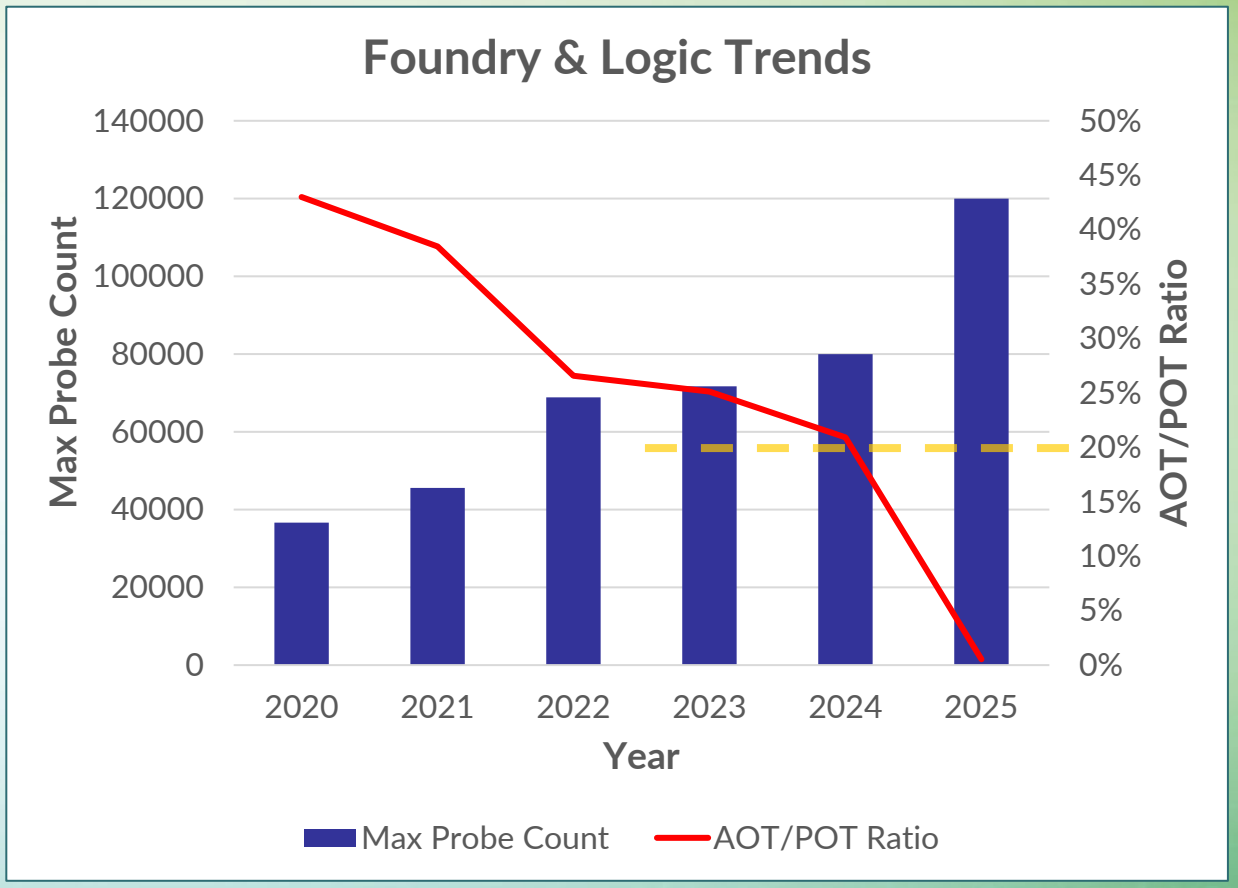
- **New packaging solutions**
  - New packaging technologies enable tighter pitches for improved PWR/GND and IO coverage
- **Power delivery performance:**
  - Increasing number of V_{dd} and V_{ss} bumps to reduce impedance and improve the power delivery network (PDN)
- **Test costs:**
  - Some customers are not increasing per DUT probe counts but instead are increasing parallelism to improve throughput

High Probe Count Trend

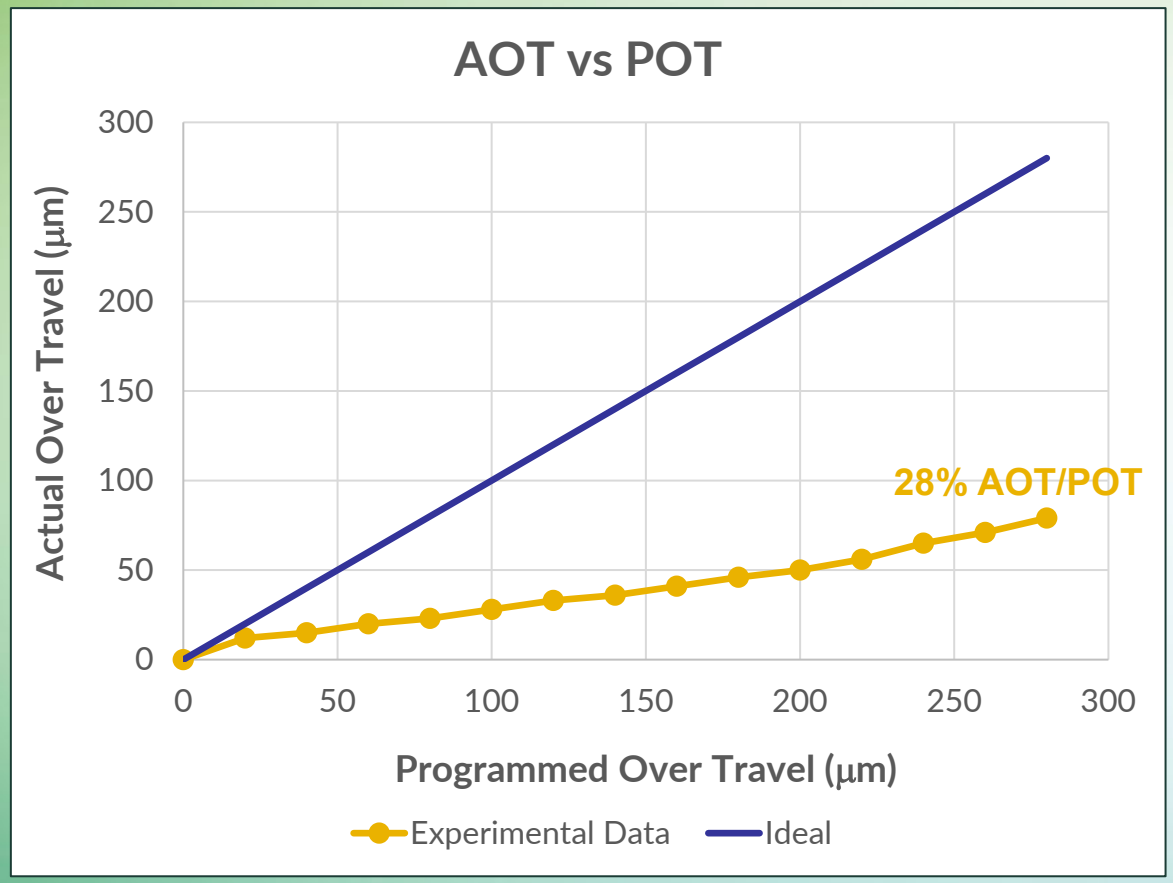
- FormFactor is shipping 80k probe designs today
- We see probe counts trending to 120k+ probes by 2025 and customers are already inquiring about 150k – 200k
- Based on the current trend, the Actual OT/Programmed OT ratio will become a key limiter!



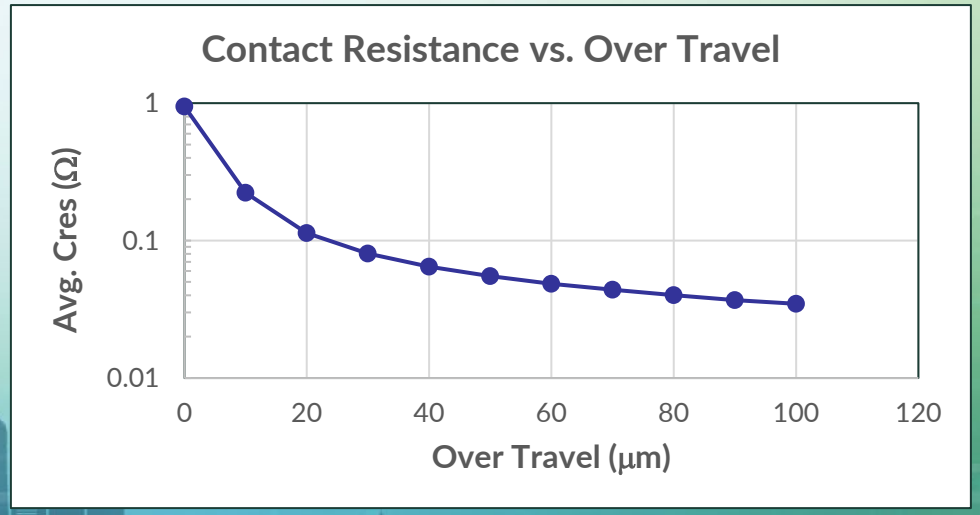
FormFactor 80k Probe Design



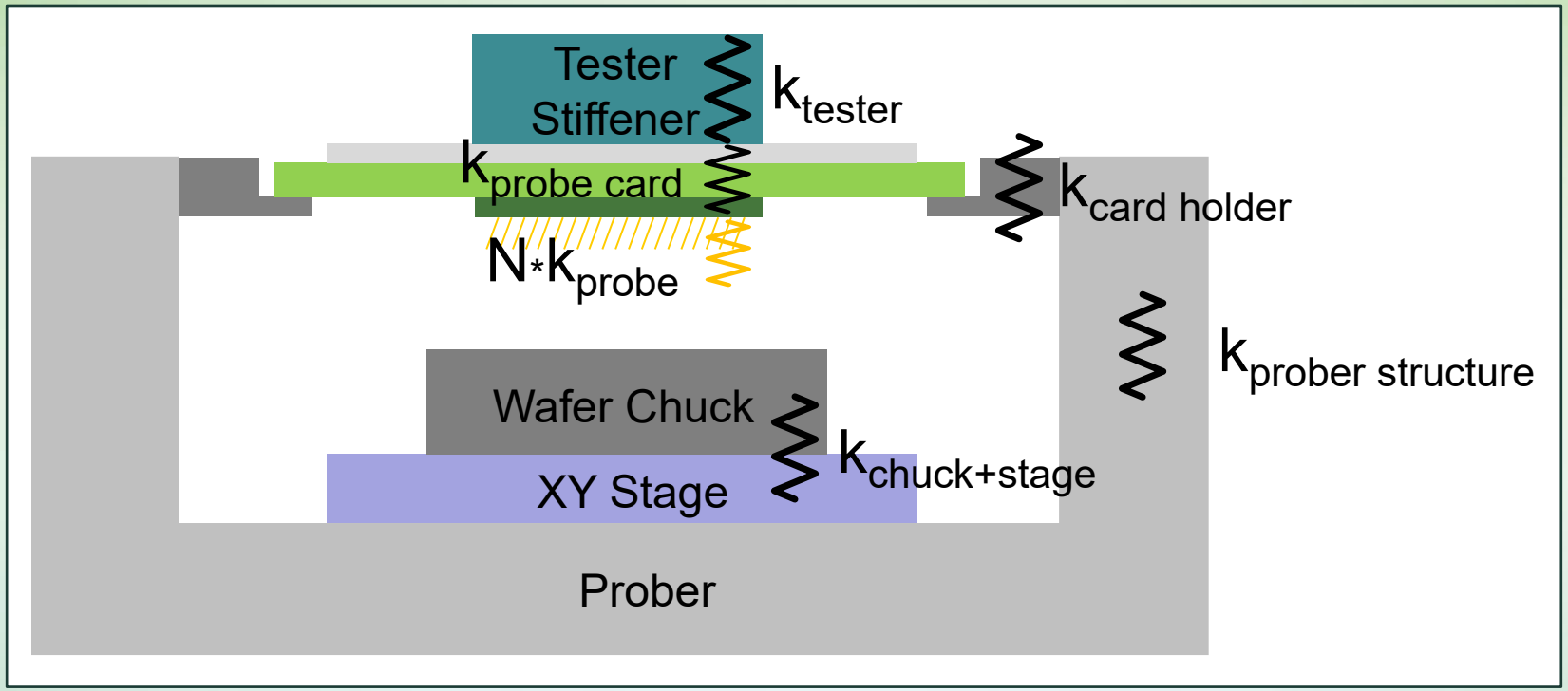
What is AOT/POT and Why Should We Care?



- **What is AOT/POT?**
  - In simple terms, the probes act as a spring and the actual compression of the probes is less than what is programmed in the prober recipe due to non-infinite system stiffness
- **Why do we care?**
  - Ultimately, we need low and stable Cres for IO performance and power delivery which depends on having adequate over travel
  - Having a high level of bow across the probe card stack-up during use leads to contact and reliability concerns for these large probe arrays



System Stiffness



Reference: T. Berry. K. Breinlinger, R. Rincon, SW Test, 2012

The system consists of a group of springs in series:

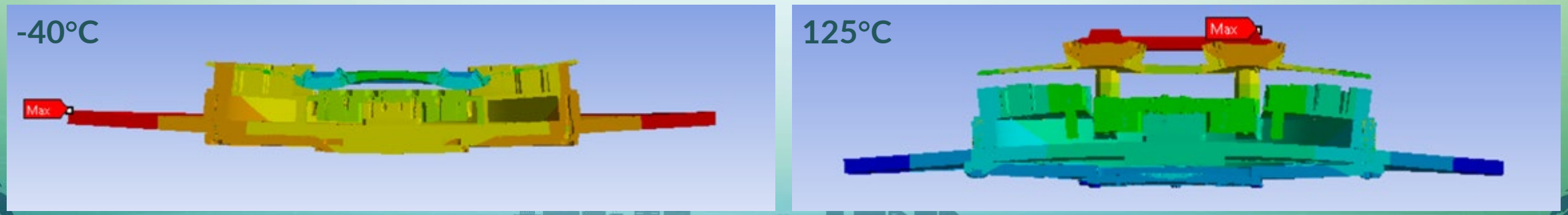
$$\frac{1}{k_{system}} = \frac{1}{k_{probe\ card}} + \frac{1}{N * k_{probes}} + \frac{1}{k_{card\ holder}} + \frac{1}{k_{prober\ structure}} + \frac{1}{k_{chuck+stage}} + \frac{1}{k_{tester}}$$

where N = number of probes

How About the Impact of Temperature?

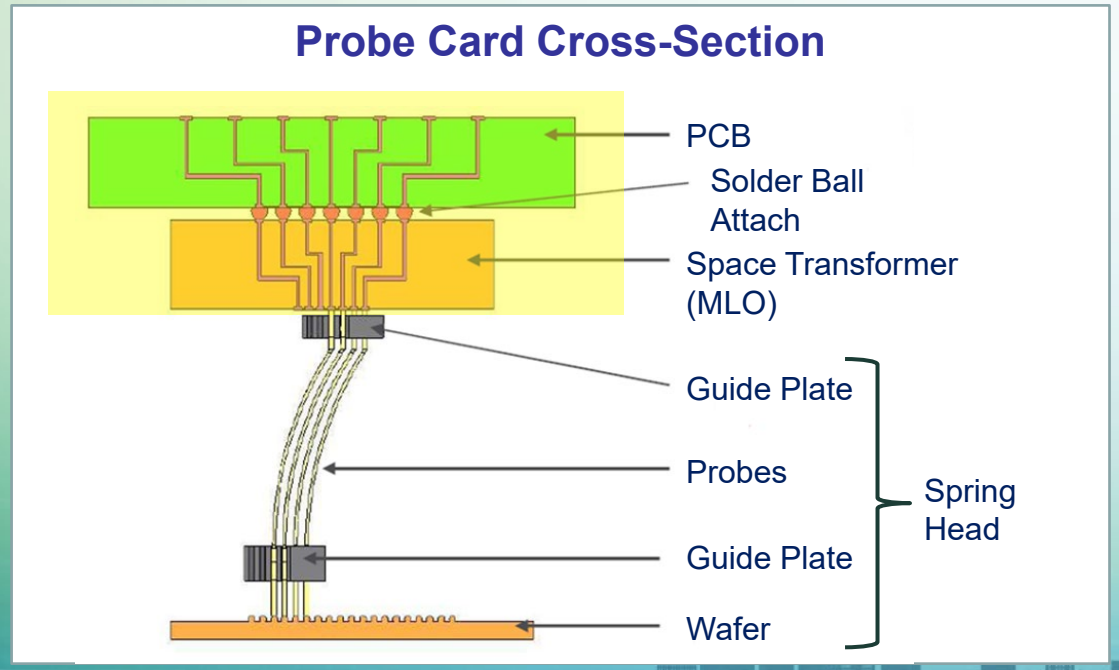
- **We know the probe card deflects based on thermal gradients and the CTE mismatch between materials**
  - Having higher probe counts will increase the contribution of thermal conduction from the wafer to the probe card and needs to be considered when designing fixturing and stiffening components
- **FEA models need to be thermo-mechanical to provide a full understanding of what is happening to the probe card during test**
- **With FFI's proprietary material selection, CTE deltas can be minimized and bow eliminated even for large arrays**

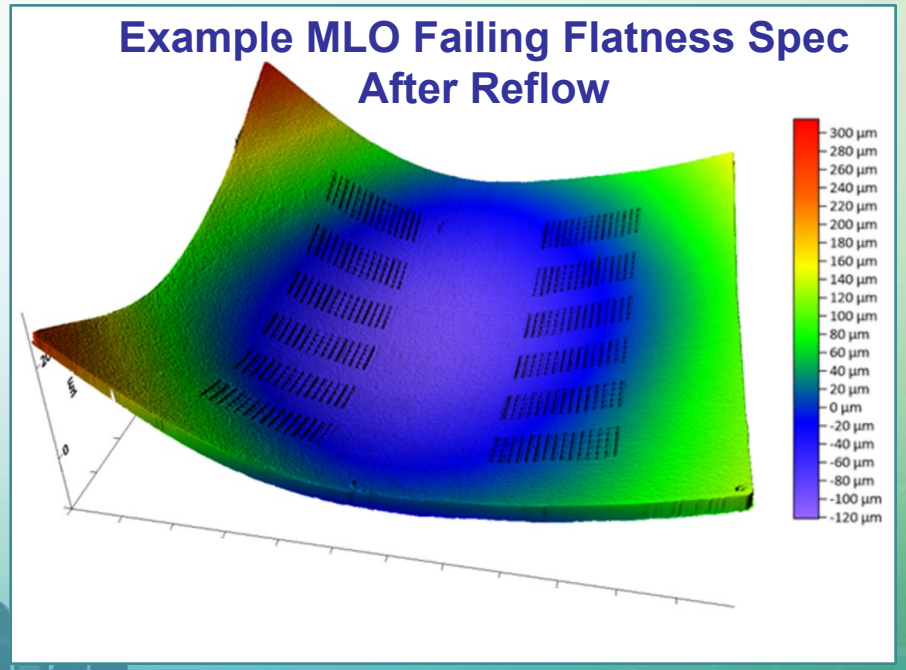
Example Probe Card Deflections at -40°C and 125°C Wafer Temperature



MLO Attach Challenges

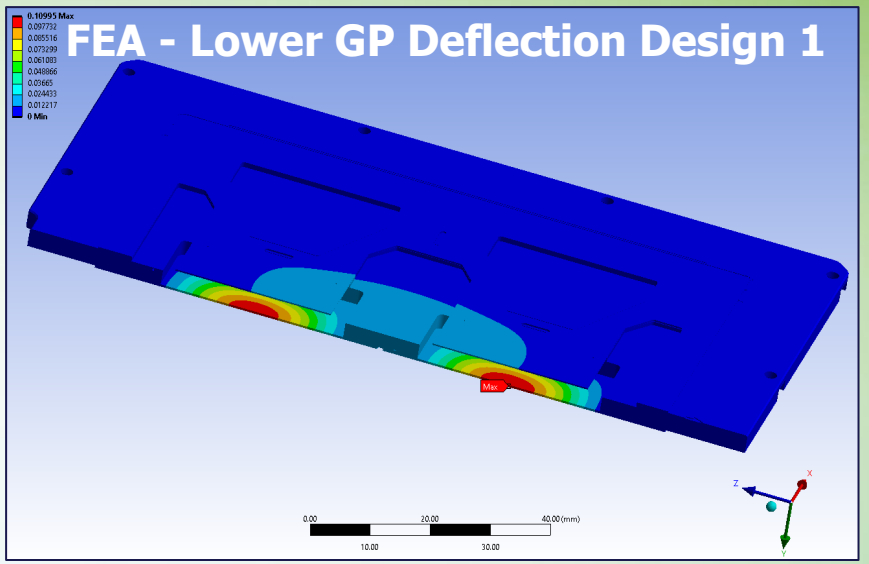
- **Larger probe arrays are requiring MLO sizes >100mm per side**
- **Major challenge is controlling bow during reflow attach to the PCB**
  - Too much bow leads to opens at the probe distal end interface to the MLO pad
- **With FFI's proprietary process, we can reflow up to 120mm MLO's without issue**

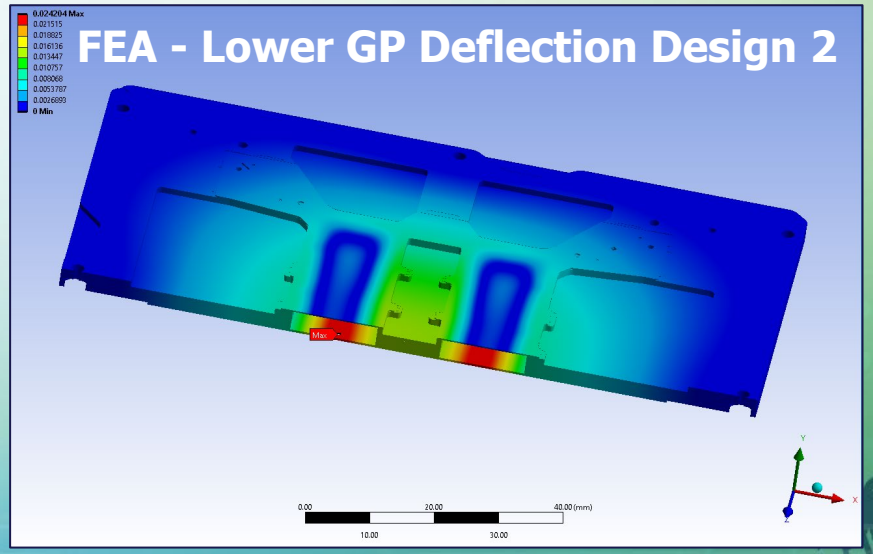




Guide Plate Material

- Probes exert lateral and frictional forces on the guide plates under compression with the lower guide plate seeing the majority of the stress
- New ceramic materials with increased bending strength are under investigation
- Alternatively, the LGP can be made thicker but at the expense of cost and lead time





Design	//	Probes/DUT	Total # of Probes	Max. LGP Deflection (μm)	Factor of Safety, Max Stress
Design 1	2	33K	66K	110	1.5
Design 2	10	5K	50K	24	7

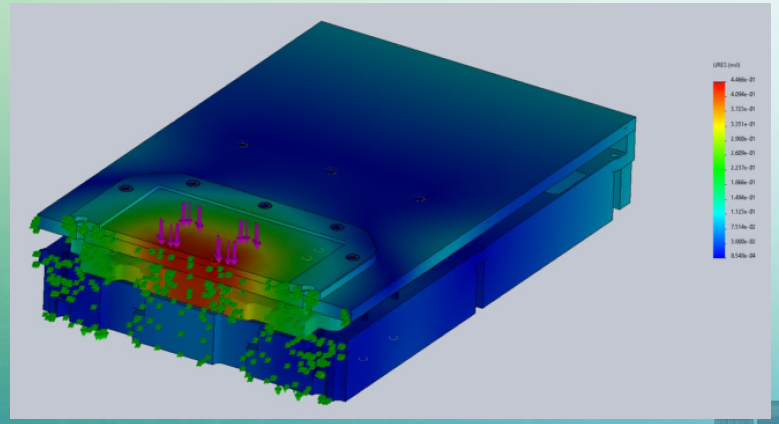
What's Needed From the Tester?

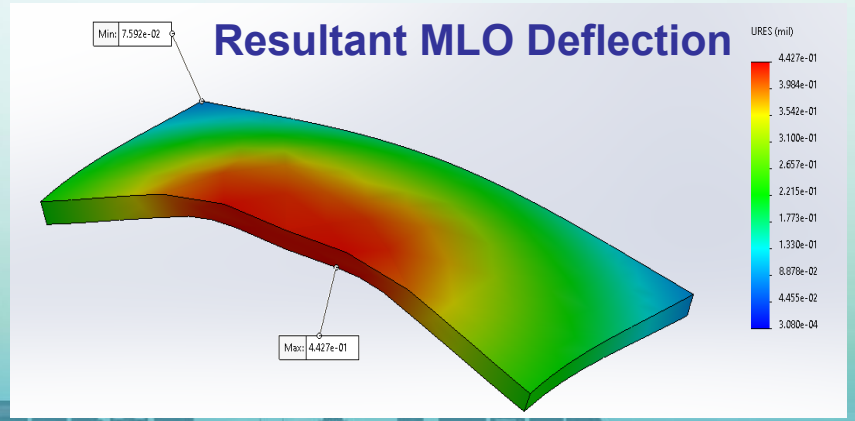
- **A stiff probe card docking interface**
- **Advantest's DUT Scale Duo Tester for example, has 3x more useable Z-height for the PCB stiffener**
  - More clearance opens up the design space for an improved stiffener that doesn't reduce component space on the PCB

Advantest DUT Scale Duo Tester

Teradyne UltraFLEXplus Tester

Probe Card Stiffness FEA Modeling

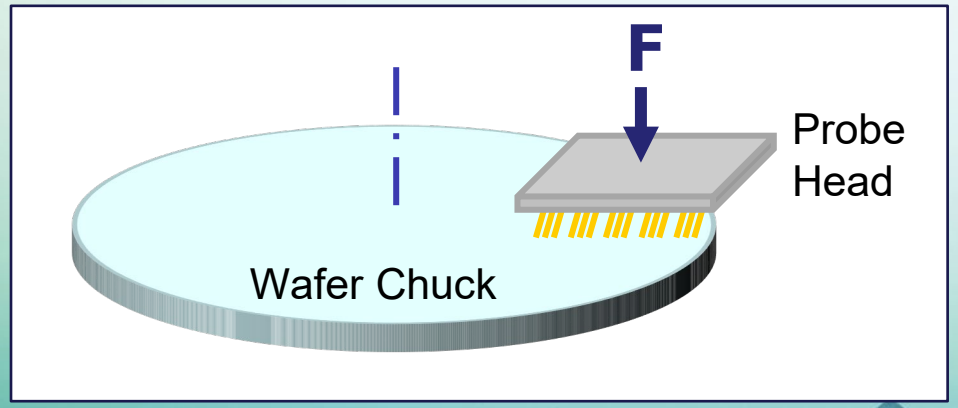




What's Needed From the Prober?

- **High force capable chucks**
  - Example: 150k probes at 2.5 gf each = 375 kg total force!
- **Minimal deflection of the wafer chuck in the offset loading condition**
- **Accretech's AP3000 prober, for example, provides chuck options up to 700 kg**

Offset Loading Condition



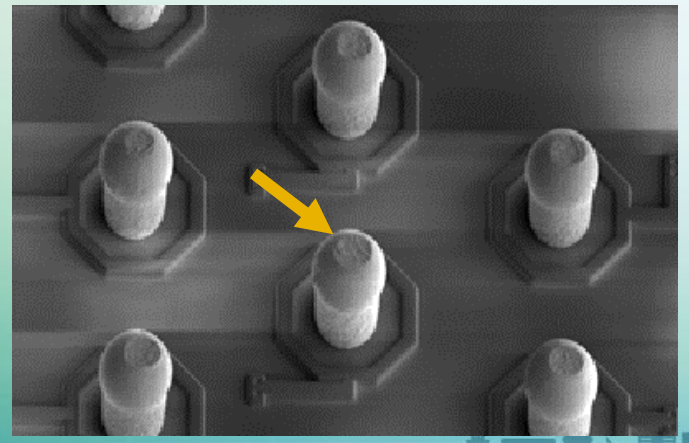
Accretech AP3000 Prober

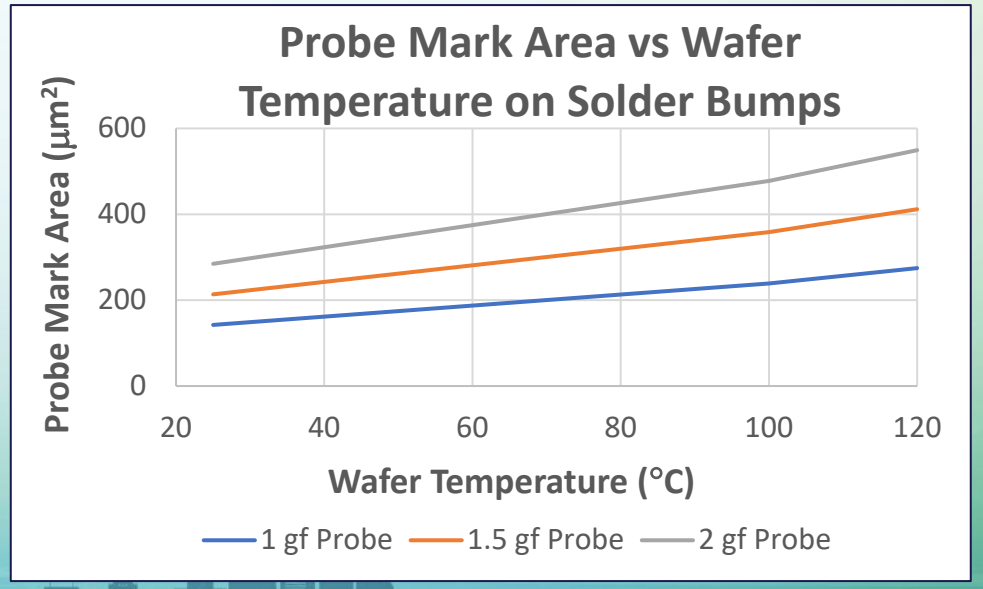
TEL Prexa Prober

The Low-Force Probe Alternative

- **An alternate solution is to introduce a low force probe to offset the higher probe counts**
- **Low force probes with high CCC are challenging to fabricate**
  - Next generation materials and fab capabilities, such as used in the FFI MT probe family, are enabling higher CCC which can be traded-off for force
- **Achieving stable Cres is also difficult**
  - What is the minimum tip pressure needed for Cres? Do higher wafer temperatures help or hurt?

Probe Marks on Solder Bumps





Summary & Conclusions

- 80k probe cards are used in HVM test today
- We need accurate numbers for the stiffness of the components in the system. The days of assuming infinite stiffness are over
  - System stiffness data collection is in progress to calibrate thermo-mechanical models
- High probe counts will challenge guide plate strength, but we have material options and will continue to search for new materials
- New testers and probers are available, promising improved stiffness
- Memory may no longer be the king of high probe counts; vertical probe cards are catching up and will surpass 100k probes

- FFI is ready for >100k vertical probe cards and are working with our partners to solve the key system challenges

Special Thanks

- Andrew Blomgren, Andrew Kontic, Doug Ondricek, David Raschko, Robert Templeton, Gideon Ukpai and many others at FormFactor