SW Test Workshop
Semiconductor Wafer Test Workshop

Break the Myth of Wafer Probing On Cu for Fan-out Wafer Level Packaging (FOWLP)

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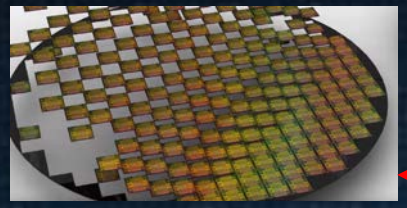
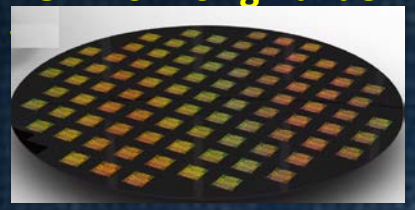
Overview

- FOWLP-Basic Definition & Advantages
- Market Trends
- FOWLP Applications
- Cu Pad Probing Challenges
- FFI Solution & Results
- Samsung Test Results
- Summary

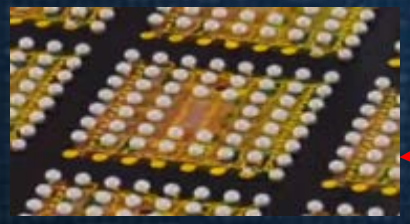
Fan-out Wafer Level Packaging (FOWLP)
Basic Definition & Advantages

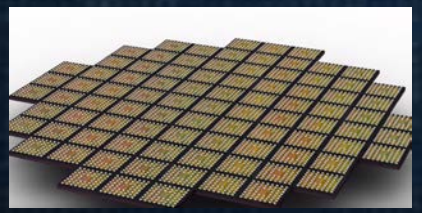


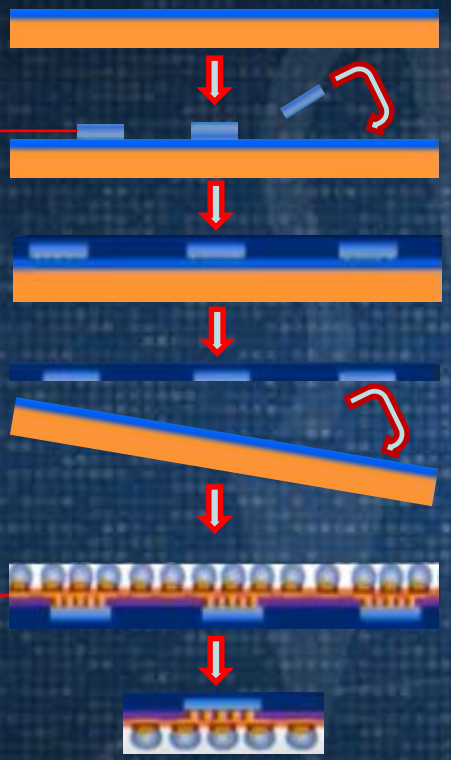
KGD from original device

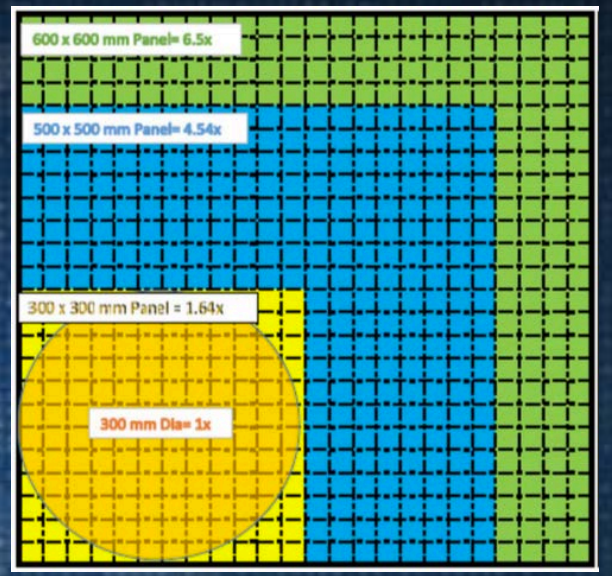


Re-constituted Wafer







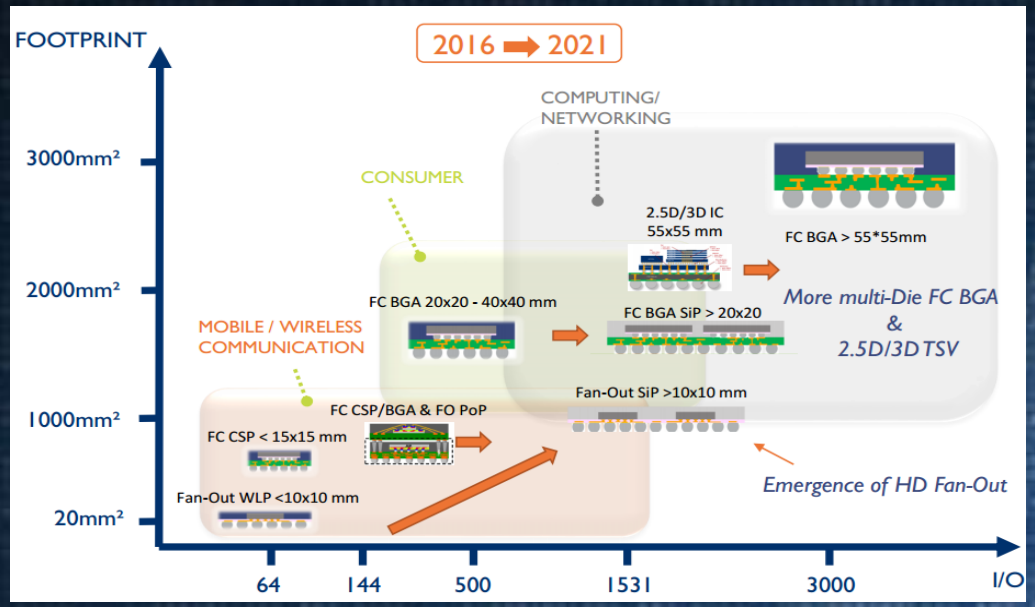


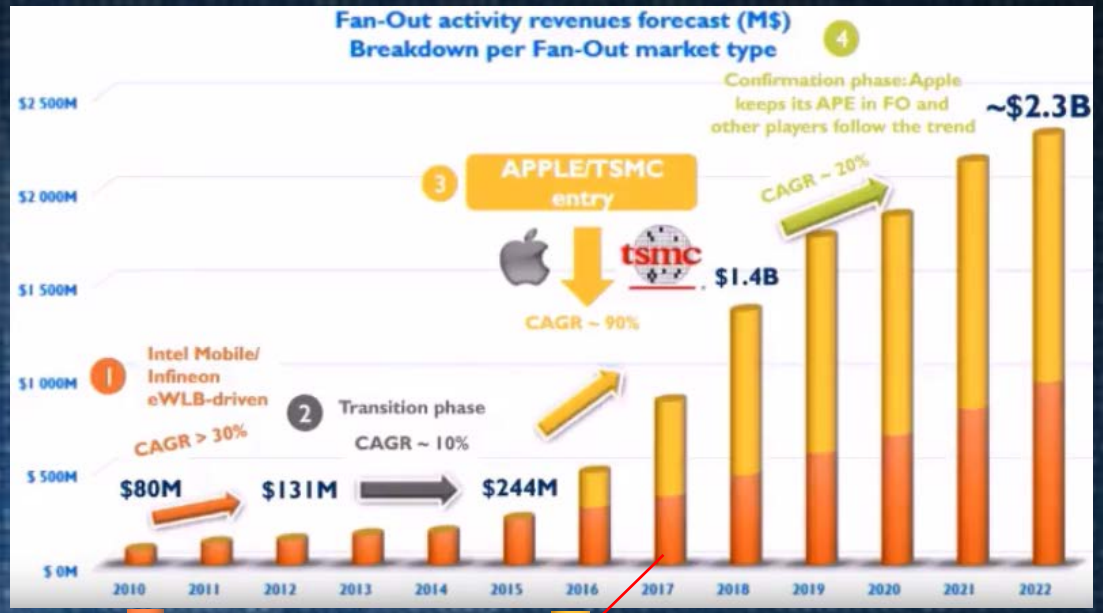
In comparison to 300mm FOWLP, alternative Fan-out Panel Level Packaging (FOPLP) provides larger processing area and lower cost per die

FOWLP Advantages Over Flipchip BGA

- Smaller Footprint & Thinner Package, no laminated substrate
- Lower thermal resistance
- Simplified Manufacturing Infrastructure
- No bump pitch restriction
- Shorter interconnections for better electrical performance

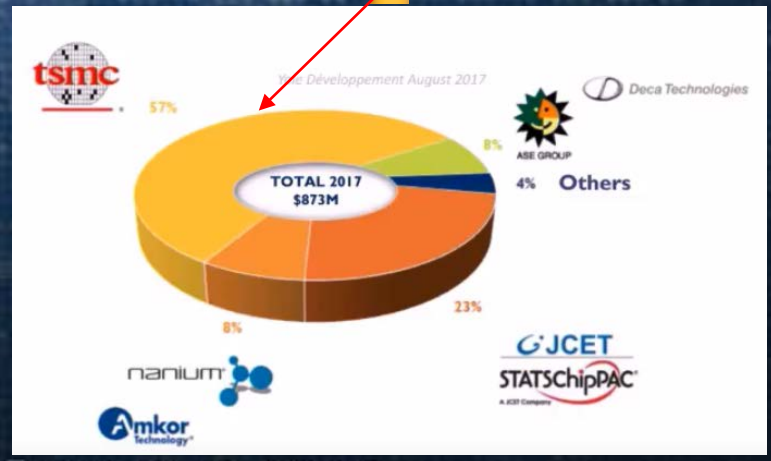
Apple Adoption of FOWLP Ignites Rapid Growth





Core Fan Out<1000 IO count

High end Fan Out>1000 IO count

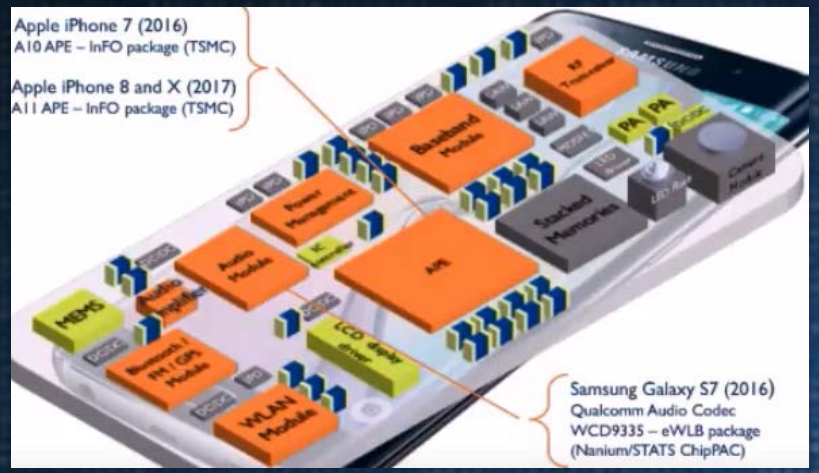


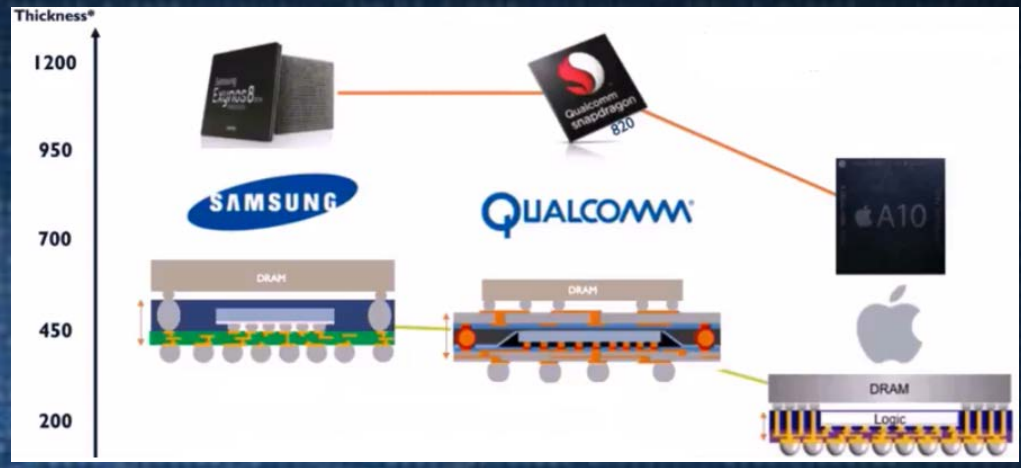
- **Market has started to grow reaching $320M in 2016 and forecasted to reach $2.3B in 2022**

Source: Yole

FAN-OUT Applications

- Application Processing Engine Applications





FOWLP Packages today

Future FOWLP

Remain on WLCSP or Flip-Chip

- Next High end
- Data centers
- Radar Applications for automotive
- Artificial Intelligence


Cisco data center switches for data centers, up to 100 Gb

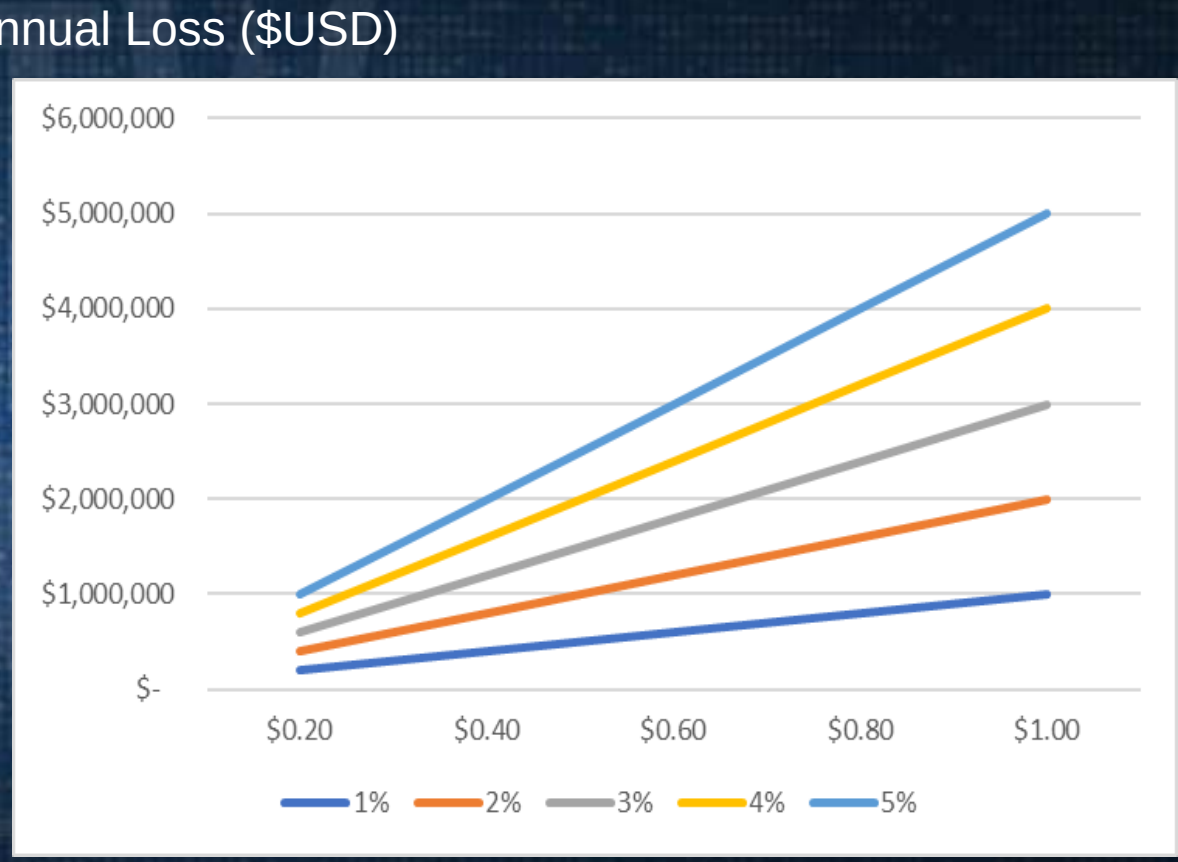

Example of Infineon's Transceiver and Receiver in Bosch MRR1 Plus Radar – eWLB packages


Nvidia P100

Source: Yole

FOWLP(FOPLP) Impact on Wafer Sort Test

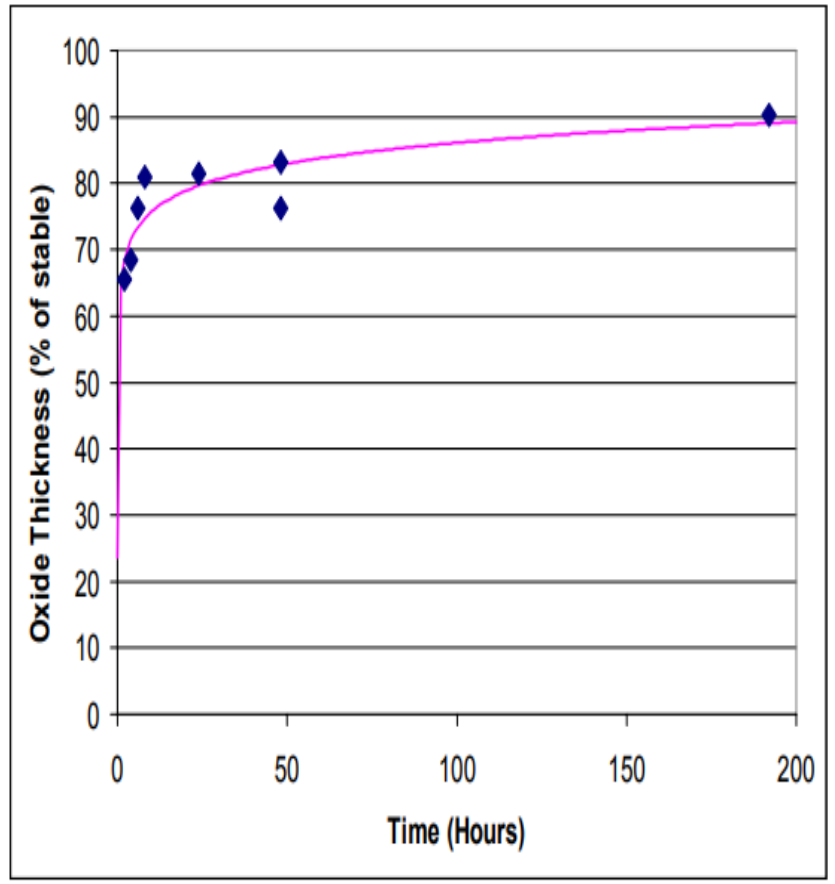
- **Known-good-die testing required to minimize the bad die going through subsequent reconstituted wafer**
- **Test on Cu Pads prior to singulation**



Perceived Challenges to Probe Cu Pads

- **Oxidation of Cu Pads even at ambient temperature**
  - Cupric oxides easily found on the pad surface (faster than aluminum oxide)
- **Cu Pad hardness greater than Al pad (Nearly doubled)**

Time (hours)	Thickness (nm)	% of final thickness
2	1.41	65.6%
4	1.47	68.4%
6	1.64	76.3%
8	1.74	80.9%
24	1.75	81.4%
48	1.79	83.3%
48	1.64	76.3%
192	1.94	90.2%
2400	2.15	100.0%



Source: Intel

Probe requirements for Cu Pad Probing

- **Adequate non-oxidizing probe metallurgy to scrub through oxide layer**
  - Avoiding probe sticking on the pad
- **Probe geometry and tip shape allowing penetration through oxide layer to have adequate scrub at optimal overtravel**
- **Stable and low contact resistance through optimized cleaning recipe**

FFI Solution

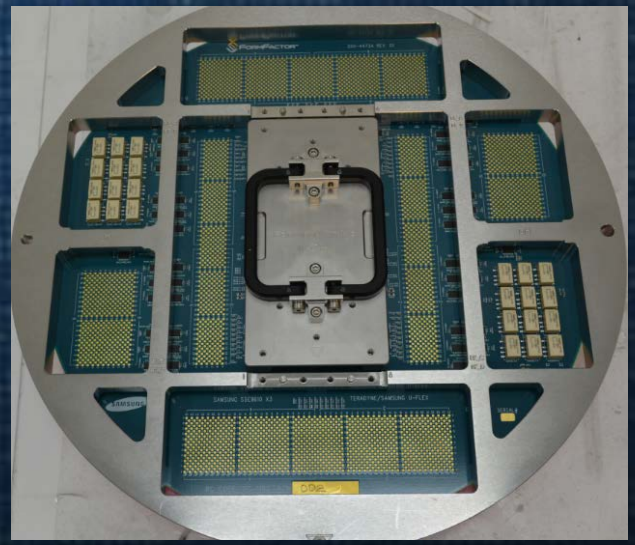
- FFI offers solution to test the known good die (KGD) that are used for Cu-Pad
- Case Study: Samsung Cu-Pad KGD tested using FFI Solution

Design Requirements

Parameters	Specification
Total number of Probes	9522
Parallelism	X3
Minimum pad pitch	90 um
Pad Material	Cu Pad
Temperature	-40C – 125C
Pad size	Octagonal 50-60um x 50-60um Uneven Topography, 30um x 30um 5um indentation

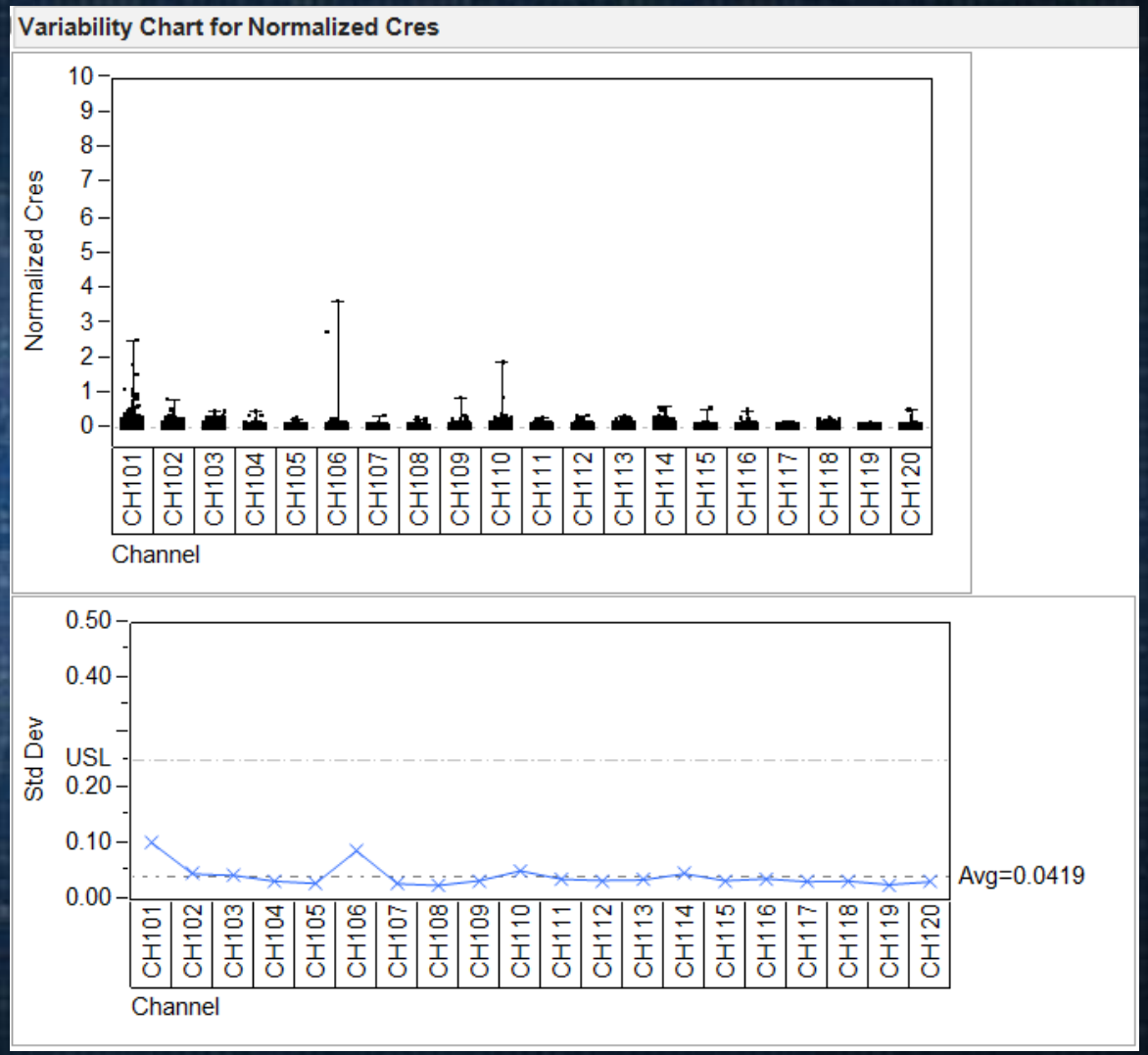
FFI Solution

Probe Type	Apollo MF80S
Minimum Pitch	80 um
Probe Force @ Recommended OT	1.5 – 1.7 g
Tip Material	Anti-wear Material
CCC	0.9A



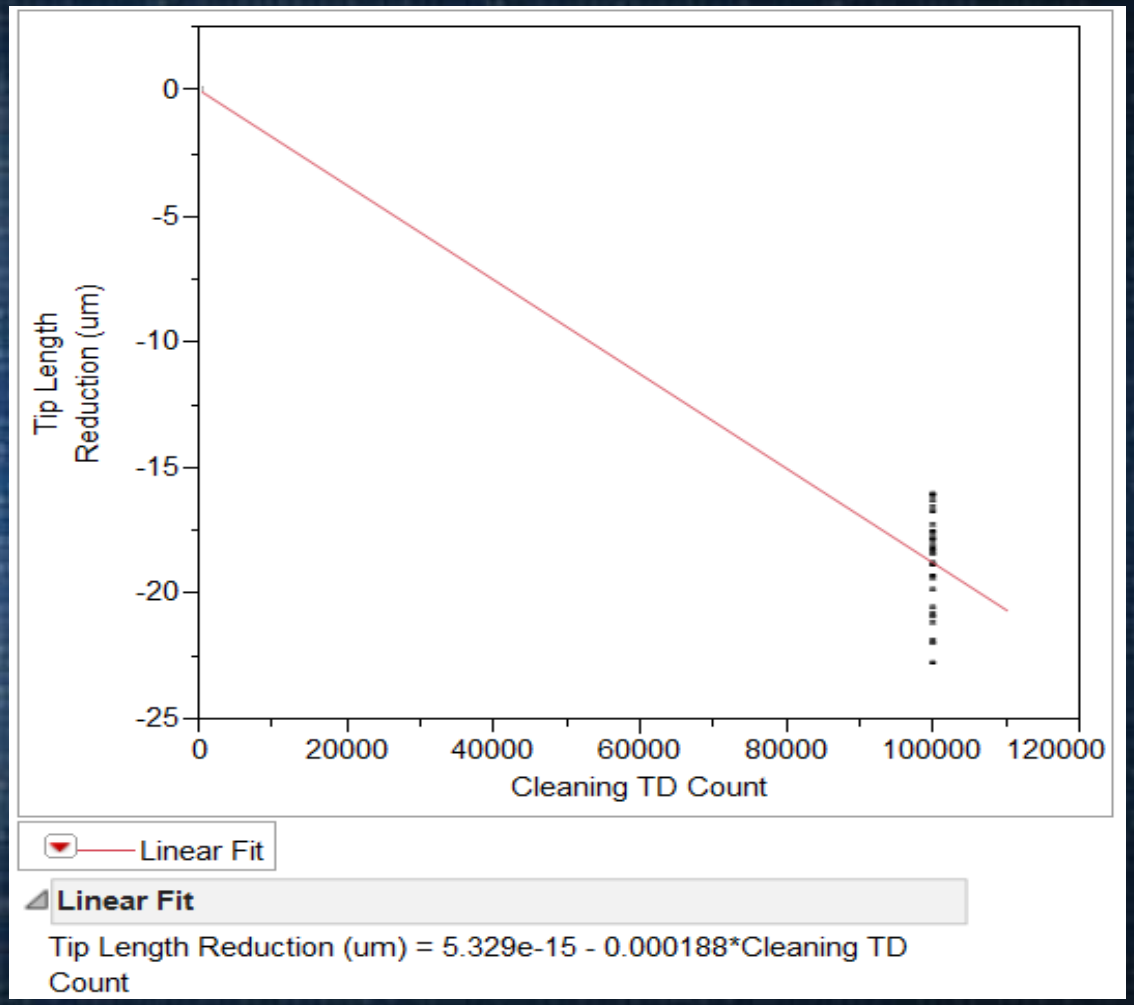
FFI Solution Internal Characterization Results

- **CRES**
  - Stable CRes on Cu wafer
  - Cres OT: 75um
  - Cleaning OT: 75um
  - Cleaning frequency:
    - 35 TD / 5 cleaning TD



FFI Solution Internal Characterization Results

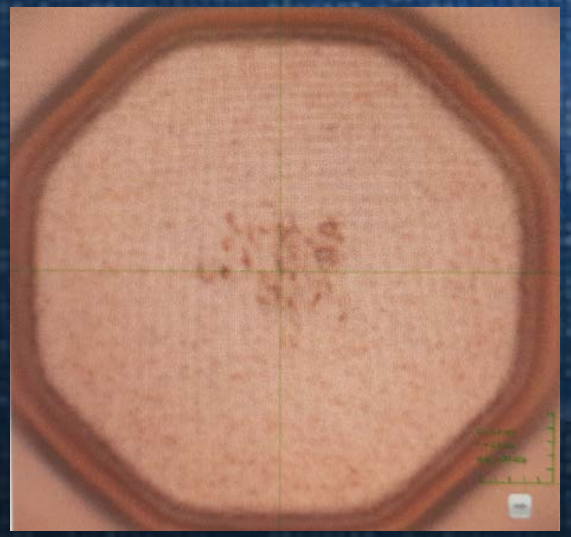
- **Lifetime**
  - Cleaning recipe
    - Cleaning OT: 75um
    - Cleaning motion: Z only
    - Cleaning media: PL-1AH
  - The average tip length reduction is 18.8um after 100,000 cleaning TDs.
  - >> 1M+ TD with 35 Cres TD/5 cleaning TD frequency.



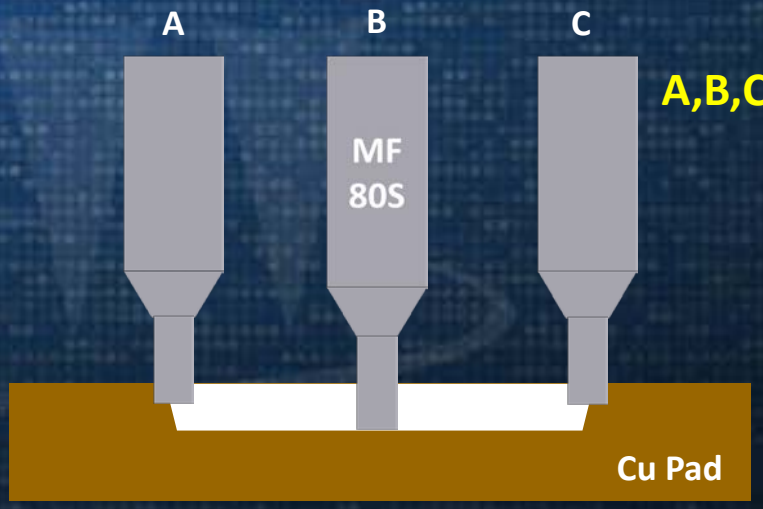
Samsung Evaluation Results

Optical Image of Samsung FoPLP Pad & Contact Mark

- **Contact mark – ok**
- **Scrub Depth : 0.3~0.4um @ 100um test O/D**
- **Probe tip is mechanically robust**
  - No broken tips when landed on the sidewall of uneven pad surface at production overdrive



Contact Mark on Dummy Pad for Evaluation



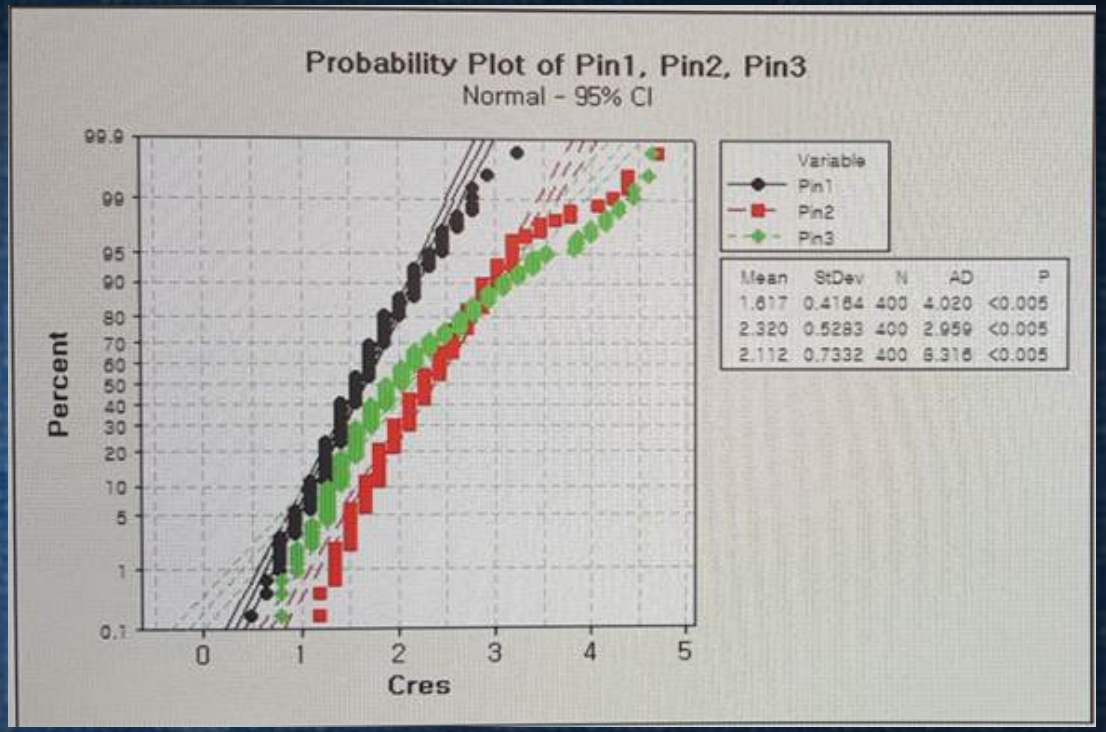
A,B,C (all) locations has no damage on RDL

No broken tip issue at probing on the sidewall of pad

Samsung Evaluation Results

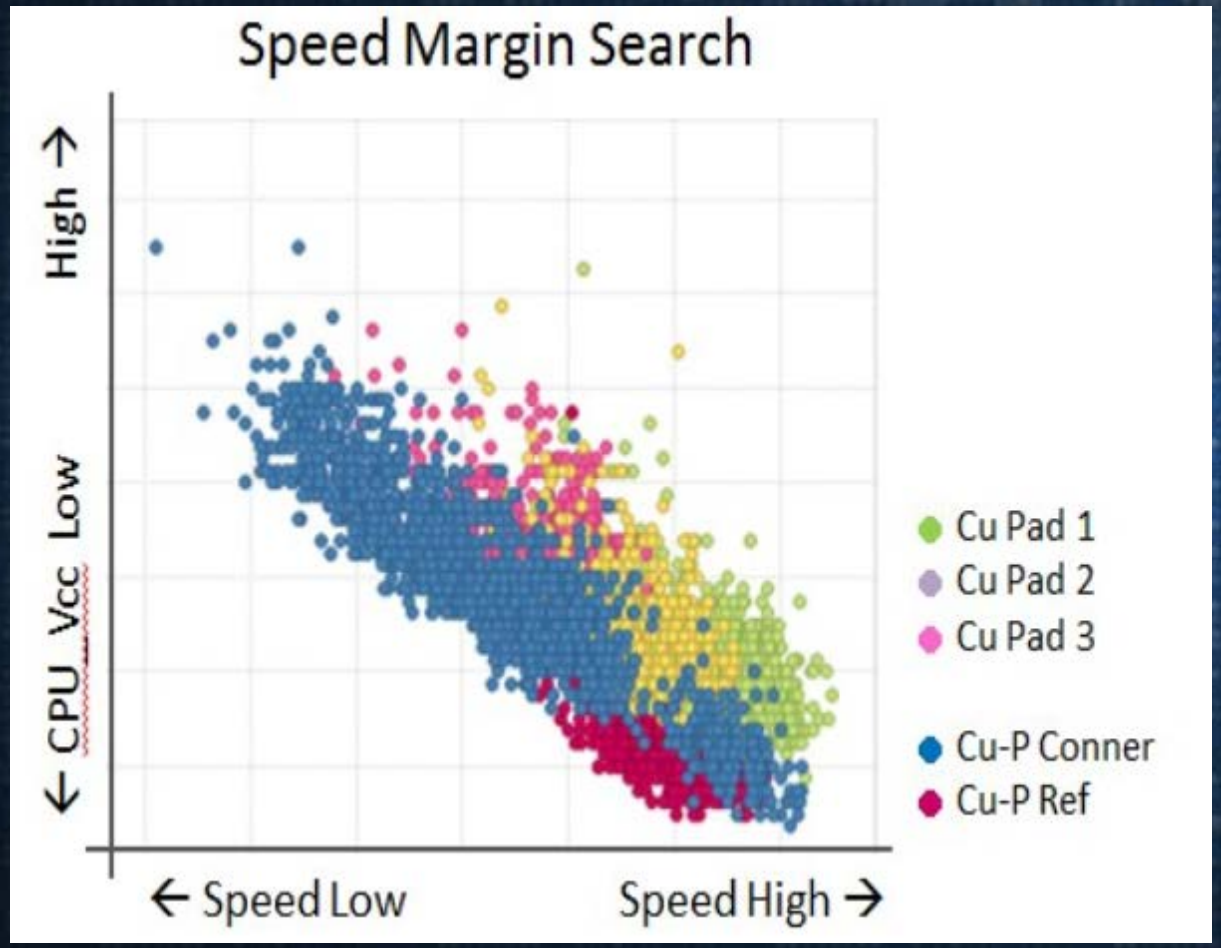
CRES Measure by Diode Curve

- Data was collected with 3 pins for 400 T/D
- Cres tends to be ~4Ω and is acceptable based on the design performance and wafer metallurgy
- Std. Dev range is between 0.4 Ω- 0.7 Ω and this range falls within Samsung spec



Samsung Evaluation Results

Function Test Margin

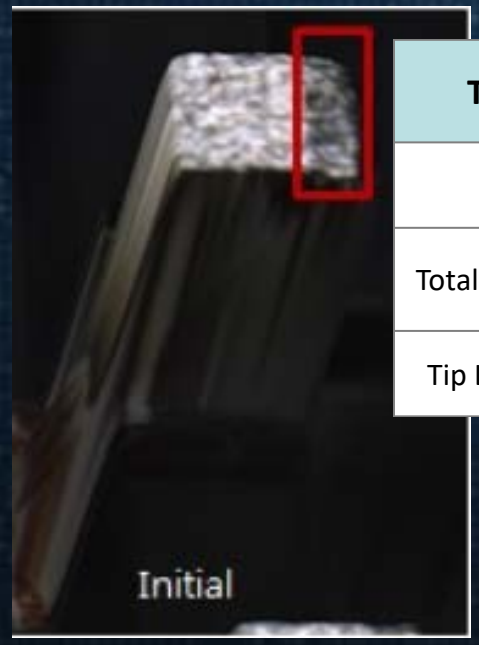


- **SEC's opinion**
  - Test results are acceptable but tip shape/size may further improve the performance
  - Target for Cu Pad is to achieve performance closer to Cu-Pillar

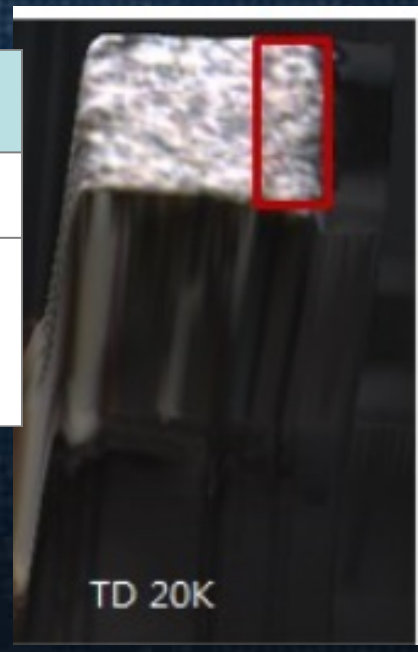
Samsung Evaluation Results

Lifetime

- T/D counted at Max. O/D & aggressive cleaning recipe
- Minimal tip wear noticed after 20K cleaning touchdowns
- Estimated lifetime 700k to 1M + touchdowns

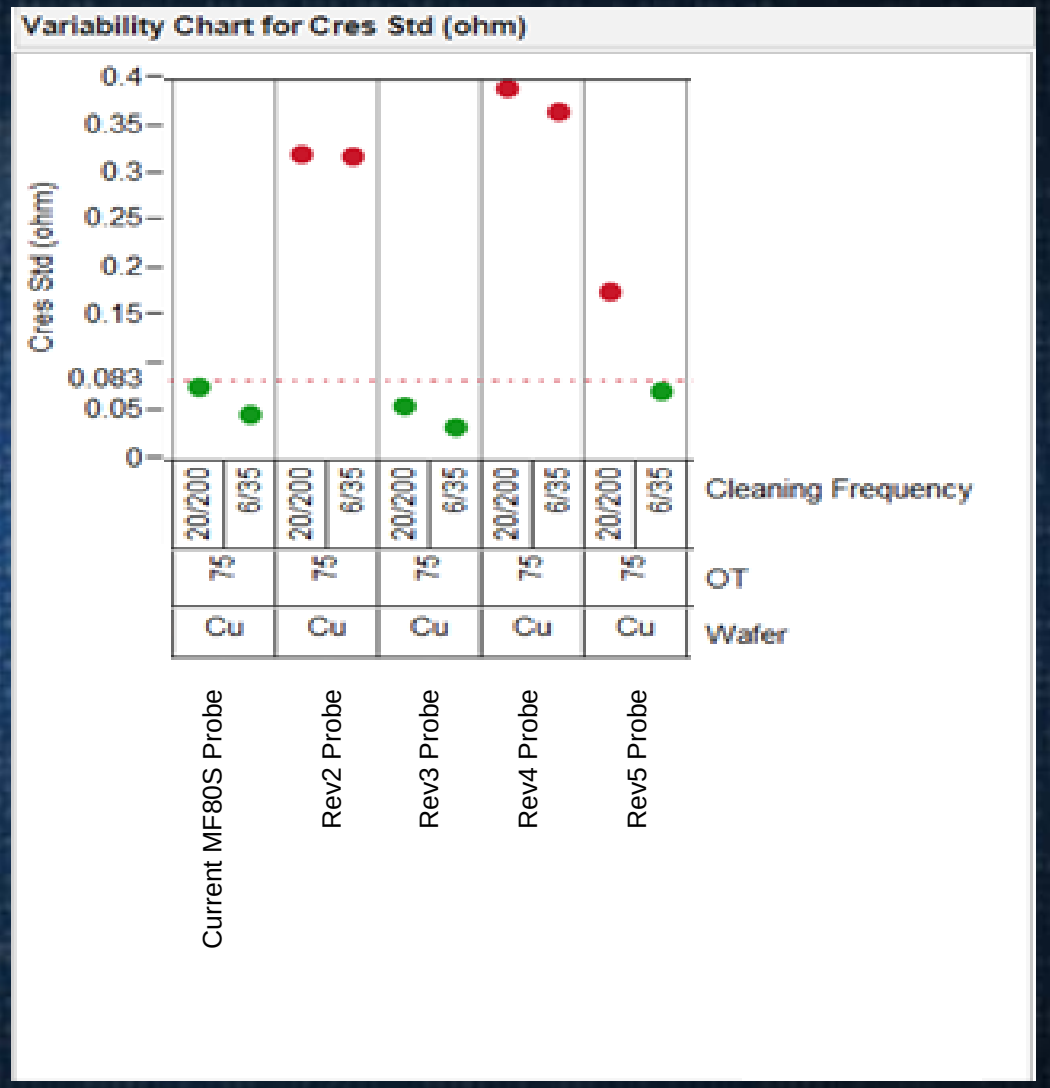


T/D	Initial		TD 5K		TD 10K		TD 20K		Review
	Min	Max	Min	Max	Min	Max	Min	Max	Initial~20K
Total Length	272	283	272	282	271	282	271	281	Worn out 1~2um (0.5um/10K)
Tip Length	106	120	107	119	107	120	105	120	



Future Work

- **CRES Study on Cu**
  - Further Improve the CRES Std. deviation
  - Optimizing Probe Design
    - Tip size and shape
  - Rev3 Probe has shown a marginal Improvement (25% Improvement)
- **Next Step is to validate the results with Samsung**



Summary

- Mechanical Robust Probe Design to probe uneven Cu Pad
- Stable and Low CRES to enable KGD testing on Cu pad
- Enabling performance closer to Cu-Pillar for chip manufacturers migrating to Cu pad KGD test before singulation for FOWLP
- Stable scrub size and scrub depth
- Higher Lifetime to reduce cost of test

Acknowledgements

- Chun-Chi Wang, Sr. Manager, Product Development (FFI)
- Jarek Kister, CTO (FFI)