



Automotive IC production wafer test in a zero-defect world

By Amy Leong [FormFactor, Inc.]



Chip Scale Review asked FormFactor's Chief Marketing Officer, Amy Leong, to respond to questions that provide insights into the challenges associated with automotive IC production wafer testing amid the requirement for zero-defects.

CSR: What are the unique production wafer test requirements for automotive ICs?

FormFactor (FFI): Semiconductor technology is key to smarter and safer cars and, ultimately, to enabling autonomous driving. According to semiconductor industry market research firm, IC Insights, the automotive IC is one of the fastest growing applications at 14% CAGR (2016-2021), and projected to reach \$43 billion by 2021. We are seeing the soaring proliferation of radar, LiDAR and image sensors to help cars "see" better; RF/mmWave chips to enable vehicle to vehicle (V2V) and vehicle to infrastructure (V2I) communications; and microcontrollers to help vehicles make more intelligent decisions in order to support an increasing level of autonomy.

These innovations in automotive semiconductor ICs post a high bar for wafer test. Due to its inherent safety requirements, automotive IC test is becoming more difficult and more time-consuming. Defect levels for automotive ICs are at least 10X more stringent than those for mobile and consumer applications, demanding parts per billion (ppb) failure rates and mandating zero-defect manufacturing. In addition, the test conditions are more extreme, such as cold temperature (-40°C) and hot temperature (>=160°C), high power (10,000V) and high current (600A) requirements. Supply chains are also getting more complex as automotive IC chipmakers globalize their production footprint. Supplier scale and sustainability now become more crucial than ever.

CSR: What is the significance of supplier scale and sustainability as it pertains to automotive ICs, and how do those attributes directly affect your solutions in this area?

FFI: Unlike mobile phones, which we often change every two to three years, a car is expected to work for more than 10 to 15 years. Once an automotive IC is designed in a car model, the entire supply chain needs to be prepared to support the chip for a very long time. In addition, an automotive IC maker can have a network of wafer fabrication and test sites across the globe. Our customers expect suppliers to provide local support wherever they test the wafer, for as long as the chip is being used in the car. Therefore, scale and sustainability are essential for a supplier to automotive IC makers.

A sustainable supply chain starts with trust. We have established 10 design centers and 22 service centers worldwide, with our latest addition being in France. For an automotive IC maker, FormFactor's support team is stationed across US, Europe and Asia, where probe card designers are close to customer chip designers to minimize design cycle-time, and service engineers are rapidly on hand to maximize uptime. We enable customer success through our technology, partnership, "First Time Right" product quality, and global customer support.

CSR: How can productivity improvements be achieved while maintaining zero defects?

FFI: Testing of automotive ICs is becoming more complex and time-consuming. The key challenge for wafer test suppliers is how to provide good enough test coverage to meet the high quality requirement for

automotive ICs, without driving up the cost of test. The biggest bang for the buck to reduce test cost is to test as many dies in parallel as possible to dramatically increase productivity.

As an example (excluding test program impacts on the actual throughput), to test a 300mm wafer with 1000 dies, if we test 10 dies at a time with a test time of 1 minute per wafer touchdown, it will take 100 minutes to complete testing of the wafer. If we can test 100 dies at a time, the total test time would be reduced by a factor of 10 to 10 minutes. At a test cell hourly rate of \$60 per hour, a reduction of test time by 90 minutes would lead to a \$90 test cost saving per wafer. At a chip design running at 20K wafer starts per month (WSPM), this would translate to an annual savings of over \$20 million—a remarkable profitability enhancement for automotive IC makers. This parallel test concept is certainly not new. It has been widely utilized for DRAM wafer test for more than two decades, and now we have extended this capability to automotive ICs, with parallelism in the range of 3000 DUTs.

Wafer probing is a "contact sport." The more force the probe puts on the wafer test pad, the greater the chance to create defects to the circuitries underneath the pad. To support a zero-defect manufacturing process, probe cards must be designed with the gentlest force possible to eliminate any chance for under-pad cracking, while maintaining a high enough force to ensure stable electrical contact and optimal test yield.

CSR: What are the design features of the TrueScale Matrix 300mm MEMS probe card that accomplish the goals referenced above?

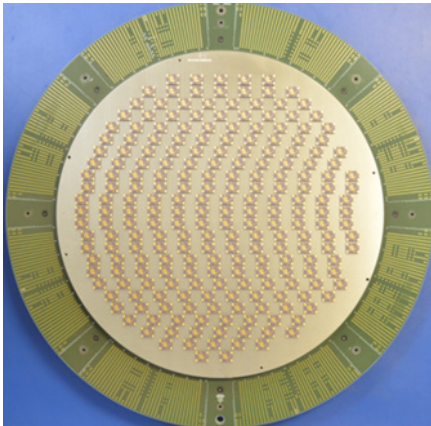


Figure 1: FormFactor TrueScale Matrix 300mm full-wafer probe card with “rainbow” touchdown pattern to maximize test throughput.

FFI: Our solution enables test cost reduction by maximizing test throughput and a zero-defect probing process by using ultra-low force MEMS probe technology that we pioneered. A few capabilities include:

1. Maximize probing area to cover the entire 300mm wafer: This provides opportunities to test as many dies as the tester channel allows, without any area limitation. In contrast, many alternative probe cards have a limited probing area of 100mm to 150mm.
2. A proprietary touchdown optimization tool to create inventive patterns to maximize throughput: As you can see in **Figure 1**, the “rainbow” pattern typically provides lower touchdowns compared to a rectangular probe card’s “solid wall” pattern. Simply put, a circular probing pattern is more efficient for a round wafer.
3. FormFactor’s proprietary TRE™ (Test Resource Enhancement) technology provides a boost to wafer test throughput: The TRE option can intelligently split a single tester resource to test multiple dies, without compromising test quality.
4. Ultra-low force design to support zero-defect manufacturing: The probe is designed with ultra-low force—less than 2 grams probe force per probe—to ensure that the active

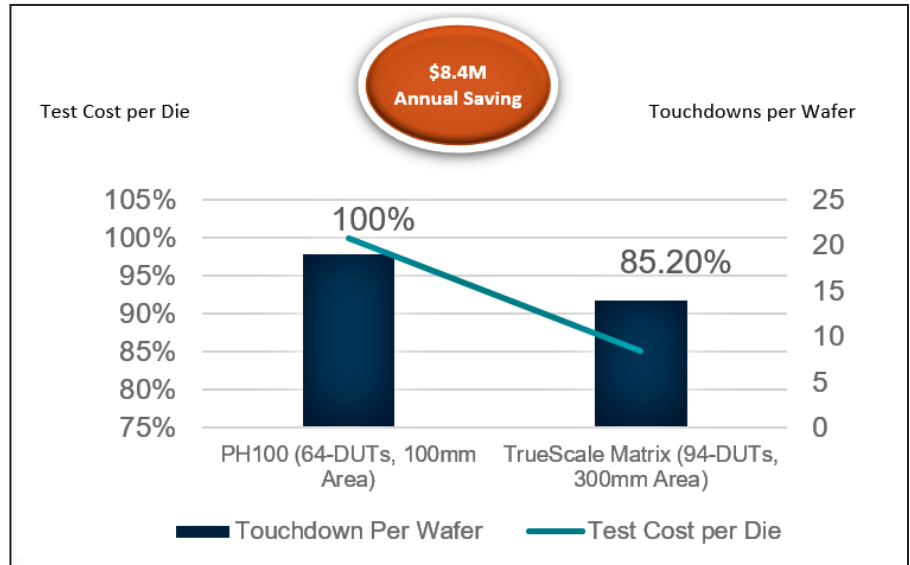


Figure 2: Automotive microcontroller wafer test cost reduction through parallel test.

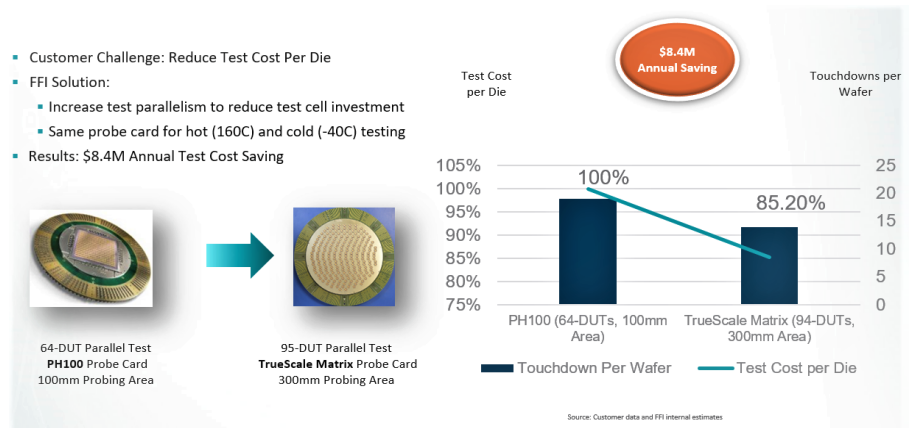


Figure 3: Case study: automotive microcontroller production test productivity improvement through high-parallelism probe card.

circuitry below the probing pad is undisturbed after multiple probing insertions at the same pad location.

The test cost reduction example shown in **Figure 2** is an automotive microcontroller (MCU) production case using TrueScale Matrix. The microcontroller is the brain for smart cars that makes rapid intelligent decisions. It is equipped with high embedded memory content, which exponentially drives up the test time and test cost compared to other digital ICs. To reduce test cost, the customer in this example used TrueScale Matrix to increase throughput from 64 devices

under test (DUTs) per touchdown to 95 DUTs, as well as optimized test patterns to further reduce touchdowns per wafer. As a result, the test cost per die was reduced by 15%, and led to an annual savings of \$8 million (**Figure 3**).

CSR: What technical challenges did FFI overcome to enable 300mm full-wafer test for automotive ICs?

FFI: As we increased the probing area to 300mm for automotive IC wafer test, a couple of new challenges emerged:

1. Control of the probe tip planarity within 30 microns to ensure stable electrical contact for every DUT:

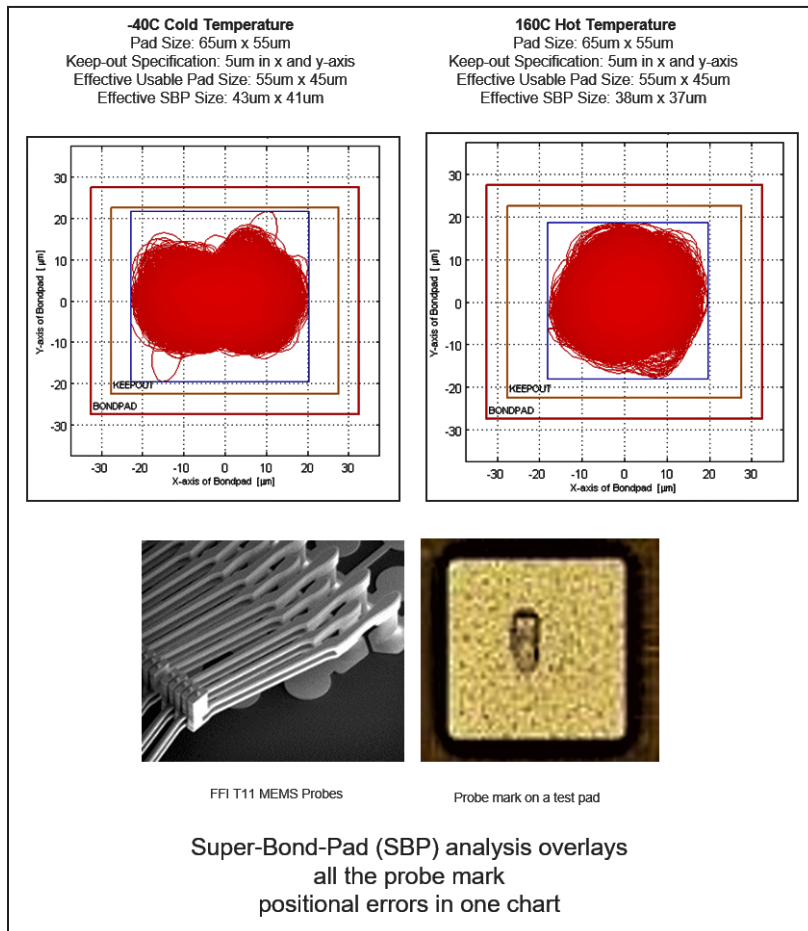


Figure 4: Super-bond-pad (SBP) analysis for an automotive microcontroller at cold (-40°C) and hot (160°C) test temperatures.

With 20,000 to 100,000 probes per probe card—even at an ultra-low force of 2 grams per probe—several hundreds of kilograms of force are exerted over a 300mm probing area. This is equivalent to having a killer whale sitting on a 12-inch large pizza, while trying to maintain the less than paper-thin flatness of the pizza.

2. Thermal expansion control over a wide temperature range:

One unique test requirement for automotive ICs is that they need to be tested at both cold (-40°C) and hot (>=160°C) temperatures. A silicon wafer has an average coefficient of thermal expansion (CTE) of 2.8ppm/°C. When testing at 160°C, a silicon wafer will expand approximately 125 microns across its diameter. Therefore,

temperatures, we measure the bounding box of each probe mark on every probe pad on the wafer, then superimpose all the measurements onto a “Super Pad.” This procedure is then repeated for cold temperatures. This approach provides a holistic view of the probe mark performance across the entire wafer over the full temperature range. As you can see in **Figure 4**, using the same probe card design, at both cold -40°C and hot 160°C, all the probe marks fall within the pad with good margin to the edge.

Biography

Amy Leong has been with FormFactor since 2012 and is CMO at the company. Prior to this, Ms. Leong was the VP of Marketing at MicroProbe—from 2010 through the 2012 closing of FormFactor’s acquisition of MicroProbe. Before joining MicroProbe, Ms. Leong worked at Gartner, Inc. (2008–2010) as a Research Director covering the ASSP system-on-chip and microcontroller markets. From 2003 to 2008, Ms. Leong worked at FormFactor where she served as Senior Director of Corporate Strategic Marketing and Director of DRAM Product Marketing. Prior to FormFactor, Ms. Leong worked in a variety of semiconductor process engineering and product marketing roles at KLA-Tencor and IBM. Ms. Leong holds an MS in Material Science and Engineering from Stanford U. and a BS in Chemical Engineering from the U. of California, Berkeley. Email aleong@formfactor.com

the pads located at the perimeter of the wafer will shift outward by approximately 60 microns, relative to the center of the wafer. In order to probe these pads, the probe card must match the 125-micron expansion. Otherwise, the probe mark will fall outside the probe pad, which is typically 50 microns in size.

TrueScale Matrix has a DUTlet architecture (i.e., tiny ceramic blocks with MEMS probes) to address critical thermal mechanical challenges. This architecture assembles a bunch of DUTlets into a wafer-side-stiffener (WSS). A variety of different WSS materials with different CTEs can be selected to match the specific thermal test conditions of each customer. This allows the probe tip to dynamically follow the probe pad as the wafer expands or contracts with temperature changes, achieving consistent probe to pad alignment (PTPA). In contrast, competitive architectures are limited to one specific CTE of the ceramic material alone—that is, one CTE for all applications.

To maintain all the probe tips at the same planar level within 30 microns, TrueScale also incorporates a tester-side-stiffener (TSS), which provides the stiffness required to counter the large system deflection as the probes touch on the wafer.

CSR: Explain the significance of the super-bond-pad (SBP) analysis.

FFI: FormFactor uses an SBP measurement to verify that the probe mark falls inside the probe pad. After probing the entire wafer at hot