Evaluation of advanced probe cards for large-array fine-pitch micro-bumps

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Vertically-stacked multi-die assemblies are a cost-attractive alternative to keep the momentum of Moore's Law going now that technology-node scaling becomes increasingly difficult and expensive. Such assemblies come in many flavors: 2.5D- and 3D-stacked ICs, fan-out wafer-level packages (FOWLP), etc. The stacked components are often large dies in leading-edge technology nodes. Consequently, their yields require testing before stacking (so-called "pre-bond test"), to prevent low compound stack yields and associated high costs. These products have in common that their inter-die connections are implemented with large arrays of fine-pitch micro-bumps. For the non-bottom dies in a die stack, these micro-bumps are the only available wafer-probe interface for pre-bond testing.

Until recently, probing large-array fine-pitch micro-bumps to get wafer-level pre-bond test access into the dies was considered "impossible;" conventional cantilever-type probe cards cannot cover the large arrays, and vertical probe cards do not offer the required fine pitch. This has changed with the arrival of advanced MEMS-type probe cards that offer large fine-pitch probe arrays that match the micro-bumps. In this article, we describe the process and results of the evaluation of such advanced probe cards at imec. For this purpose, we have manufactured dedicated micro-bump test wafers and developed and installed inside our ø300mm Fab-2 clean room a new test system with dedicated hardware and software.

Probe targets

Today's most challenging micro-bump probe targets are specified by JEDEC memory interface standards: High-Bandwidth Memory (HBM2) has the largest array (~4,900 micro-bumps) and

Figure 1: JEDEC's WIO2 micro-bump array [1].

Wide-I/O Mobile DRAM (WIO2) has the finest pitch (40µm). In our experiments, we have used WIO2, as it has the most aggressive pitch. A WIO2 interface (Figure 1) consists of four banks of 73×6 = 438 micro-bumps each (hence, a total of 1,752 micro-bumps) with bank gaps of two rows and 24 columns [1].

Imec's process-of-reference (PoR) micro-bumps at 40µm pitch are representative for the industrial state-of-the-art. The landing bumps are made of copper, have a diameter of 25µm, and a height of 5µm. The top bumps are made of copper, nickel, and tin, have a diameter of 15µm, and a height of 5+1+3.5 = 9.5µm.

For characterization purposes, imec designed dedicated test wafers containing only micro-bumps which are all shorted by an underlying blanket copper layer. We named the die design "BMB:" blanket micro-bump. Each of these ø300mm wafers contains over 9.4M probe-target micro-bumps, in addition to dummy, identification, and alignment micro-bumps. The 93 dies per wafer contain, among others, 27 WIO2 arrays. We have manufactured these BMB wafers with micro-bumps varying in diameter and metallurgy, including our PoR micro-bumps.

Automatic test system

The automatic test system we have built up for micro-bump probing in the clean-room of imec's Fab-2 in Leuven (see Figure 2) consists of the following components: 1) test instrumentation consisting of a digital multi-meter and a wide switch matrix, contained in 2) a hard-docking test head with manipulator, which connects through an interface with spring-loaded contacts to 3) an advanced MEMS-type probe card, which is placed in 4) a fully-automatic probe station with wafer loader; the system is completed by 5) in-house developed software for automatic test generation and result data visualization and analysis. The various system components are described in more detail below.

The probe station is FormFactor's fully-automatic Cascade CM300 in dual configuration, i.e., two probers sharing a central material handling unit (MHU), a.k.a. "auto-loader." The two probers are largely identical. Both can automatically load wafers from the shared MHU, but also have a front-side manual load port that accepts ø200mm and ø300mm wafers as well as large SEMI G74-0669-compliant tape frames for wafers up to ø300mm [2,3].

Figure 2: Test system for evaluation of micro-bump probe cards installed in Fab-2 at imec.

Both probers feature an anti-vibration table, a thermally-controlled wafer chuck (between –60 and +200°C), and a general-purpose interface bus (GPIB) command interface. The probers support vertical, non-see-through probe cards through software overlay of the wafer image from the downward-looking platen camera and the probe-card image from the upward-looking chuck camera.

The left-hand prober has been adapted to work in conjunction with a hard-docking test head. To make space for the test head, the default microscope bridge and top-view camera have been removed. Fortunately, the (also downward-looking) platen camera is still available. A Reid-Ashman manipulator lifts the 165kg test head and allows it to gently lock into the docking mechanism on the probe station. Once docked, the tester channels connect to the probe card via a spring-contact interface.

The test instruments are based on National Instruments' (NI) PXI series. An NI STS T2 test head holds two PXI racks. Rack 1 is primarily used for parametric and functional testing, while Rack 2 is dedicated for WIO micro-bump probing. Rack 2 contains a PXI-4072 digital multimeter (DMM) that drives nine concatenated PXIe-2535 switch matrix modules, constituting a wide switch matrix with 9×136=1,224 output channels. These output channels ultimately connect to probed micro-bumps and by appropriately configuring the switch matrix, we can allow the DMM to perform two- and four-point resistance measurements between any of the micro-bumps.

The probe card routes the test signals to its center, where we are employing as probe head a Pyramid Probe® Rocking Beam Interposer (RBI) "probe core" from FormFactor (see Figure 3). A probe core is a rectangular metal frame with a "plunger"" that sticks face-down through a rectangular hole in the probe card and touches the wafer. On its four outer edges, the probe core makes electrical contact to little pads on the probe card. A thin-film membrane patterned with conductive traces is attached across the plunger and serves as a space transformer between the core-I/Os and the dense array of probe tips. The RBI probe tips are part of a coupon of a second thin-film membrane, which is affixed on top of the aforementioned space transformer membrane. The tip area is $6\times6\mu m^2$. As the probe tips rock during wafer contact, the actual physical contact to the wafer is made only by the "heel" of the tip, which gives probe marks of $\sim6\times1\mu m^2$ (see Figure 8).

Imec developed in-house software, both for automatic generation and operation control of the tests, as well as for test data analysis and visualization. A test executive program in LabVIEW controls the NI test instrumentation and, through GPIB commands, the Velox operating system of the Cascade CM300 prober. Test programs are generated automatically based on input files describing: 1) the test system, and 2) the requested measurements for the device-under-test (DUT). The former remains stable over time, while the latter are chip-design specific. The test system description is essentially a look-up table that associates the various probes, via core-I/Os and spring-loaded contacts, to output channels of the wide switch matrix. From these inputs, the test generation software creates a list of switch matrix settings that connect the DMM channels to the proper probe tips. Typical measurements are two- or four-point resistance measurements between specified micro-bumps (that respectively, include or exclude the parasitic resistances in the test system itself), and the so-called "probe-check" routine (see sidebar, "Probe check routine").

The system's raw measurement data consists of a list of time-stamped resistance values R (in Ohms). These resistance values R are classified as: 1) pass ($R\leq R_{threshold}$), 2) fail ($R>R_{threshold}$), or 3) open ($R>R_{max}$), where $R_{threshold}$ is determined via a cumulative distribution function (CDF) plot and R_{max} represents the measurement range. Typically, we extract large amounts of raw data out of even a single wafer, and so there is a need to abstract and visualize that data. Our software in LabVIEW and Excel generates wafer maps, micro-bump maps, probe maps, core-I/O maps, and spring-contact maps of single touch-downs, as well as aggregate versions of such maps for multiple touch-downs. These maps are "clickable" to allow the user to drill down during data analysis. While for the evaluation of a new probe card, the probe maps are most interesting, core-I/O maps and spring-contact maps allow us to monitor the health of the test system itself. A probe map can, for example, be used to identify a probe that consistently does not make

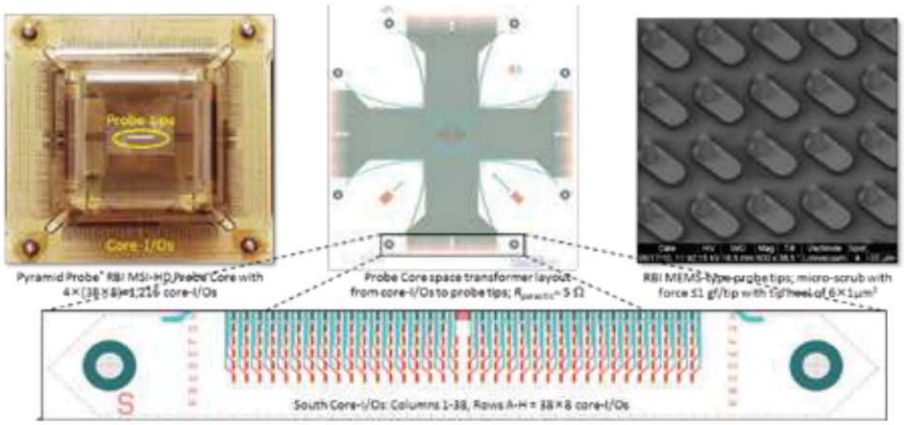

Figure 3: FormFactor Pyramid Probe® RBI "probe core:" from core-I/Os via the space transformer to the probe tips.

Probe check routine

This routine checks for every probe in a given probe set P whether it makes proper electrical contact to the wafer. In an iterative loop over all probes $p \in P$, a two-point resistance measurement is performed between probe p and all other probes ($P\backslash\{p\}$) ganged. These measurements require that all probes are electrically shorted, e.g., by probing on a blanket conducting wafer or on a dedicated "probe check short" structure on a patterned wafer. Our BMB wafers are perfectly suited for the probe-check routine, as all their micro-bumps are shorted. The measurement results include the parasitic resistances of the connections in the test system and probe card from the DMM to probe p, but, provided $P\backslash\{p\}$ is large enough, excludes the parasitic resistances of the connections in the test system and probe card from the DMM to all other probes.

contact, e.g., because it's tip sits higher than its neighbors, the tip needs to be cleaned, or there is an open contact in the space transformer. A core-I/O map can be used to identify opens or poor contacts at that interface. A spring-contact map can, for example, be used to identify non-functional spring-loaded contacts, a tilted test head, or an issue with the dock's locking mechanism.

Probe card evaluation results

The purpose of wafer probing is to make a proper electrical contact, through which the die in question can be tested. Our incoming inspection procedure is performed routinely on new probe cores that arrive at imec. It consists of an iterative execution of our probe-check routine on a blanket copper wafer while increasing the chuck over-travel from 0µm (= first physical contact) to the maximum as specified by the probe-core supplier. This procedure identifies possible mechanical and/or electrical issues with the new probe core, if any, and allows us to confirm the supplier-specified recommended chuck over-travel.

Figure 4 shows the results from the incoming inspection of a WIO2-1Bank probe core with 438 probes, for which the maximum over-travel was specified at 150µm. As can be seen, this probe core operates as expected. It starts making contact at 40µm over-travel and reaches its best electrical contact at 80-150µm over-travel. At 150µm over-travel, R_{avg}=20.6 Ohm; most of this is the parasitic resistance in test instrumentation, cabling, probe card, and probe core (with σ=2.1 Ohm, mainly on account of resistance variation due to the module number of the selected output channel of the wide switch matrix).

We successfully used the FormFactor Pyramid Probe® RBI probe cards with the test system on our BMB wafers with micro-bumps of various diameters and metallurgies. The first thing we wanted to check was if the probe tips indeed landed on the micro-bumps. As depicted in Figure 5, we analyzed this by taking scanning electron microscope (SEM) pictures of probe marks at all four corners of the micro-bump array at diverse wafer locations. Ideally, the probe marks are in the center of the micro-bump. For each probe mark, we determined how far it is off-center by measuring its (x,y) coordinates relative to the center of its micro-bump. The probe-top-pad alignment (PTPA) accuracy is affected by both the probe station and the probe core. We attribute the misalignment in the bottom-left corner of the probe array to the probe station, as that bottom-left corner was the focus of the probe station's probe-card training. The PTPA inaccuracy caused by the probe station varies with the chuck position, and therefore is depicted in a wafer map. Next, we translate the four coordinate pairs such that the bottom-left corner matches the center of its micro-bump. The remaining misalignment of the other three corners indicates to what extent the probe core's tip array is off with respect to the micro-bump array grid.

Figure 6 shows PTPA accuracy results achieved on BMB wafers with a WIO2-1Bank probe core; the misalignment is separated out for probe station and probe core. The probe station is rather accurate: over the entire wafer chuck, the maximum error is 2.5µm. The probe core tips are positioned very accurately: over the entire array, the maximum error is 1.33µm (top-left corner). Note: such satisfactory results require regular calibration of the prober's chuck positioning system and usage of the prober's thermal-control system to keep the system and test wafers at a constant ambient temperature.

Electrical measurement results depend strongly on what type of measurement is requested and on the metallurgy of the to-be-probed

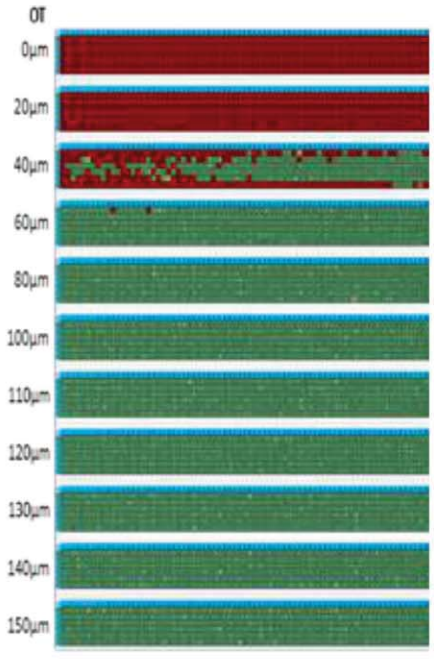

Figure 4: Probe map results of incoming inspection for a WIO2-1Bank probe core.

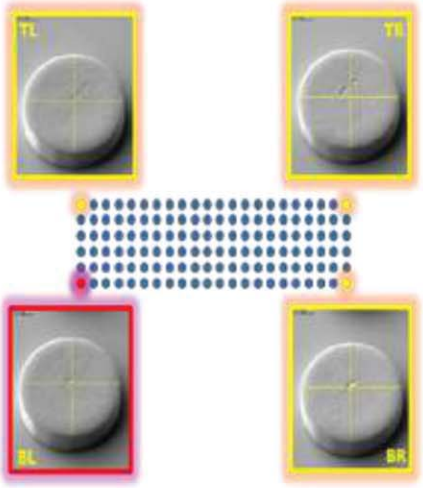

Figure 5: Approach for attribution of probe misalignment to 1) the prober's inaccuracy at specific chuck locations, and 2) the probe core inaccuracy.

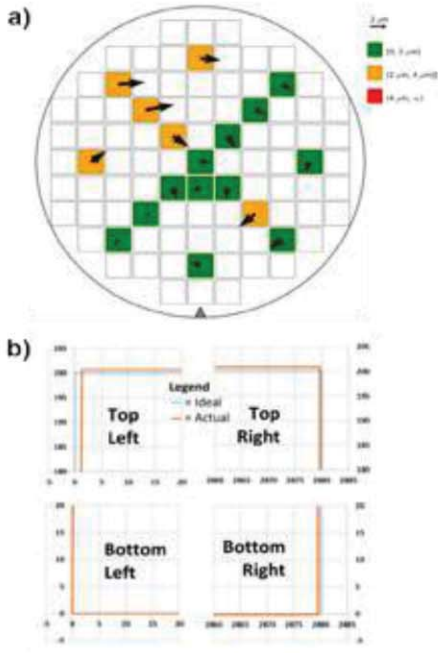

Figure 6: Measurement results of probe-mark misalignment due to: a) the CM300 prober's inaccuracy at specific chuck locations, and b) inaccuracy of the WIO2-1Bank probe core.

micro-bump surfaces. Example results for various wafers are depicted in Figure 7. The type of measurement determines which parasitic resistance contributions from the test system itself are included in the measurement result. For a two-point measurement, all parasitic resistances are included in the measured resistance value. Typically, these parasitic resistances are significantly larger than the resistance of the micro-bump to micro-bump connection through the wafer – cfr. the large green arrow in Figure 7. And then there is the contact resistance between probe tip and micro-bump. The latter is small, but unmistakably varies with the metallurgy of the micro-bump's probe surface – see the smaller purple arrows in Figure 7.

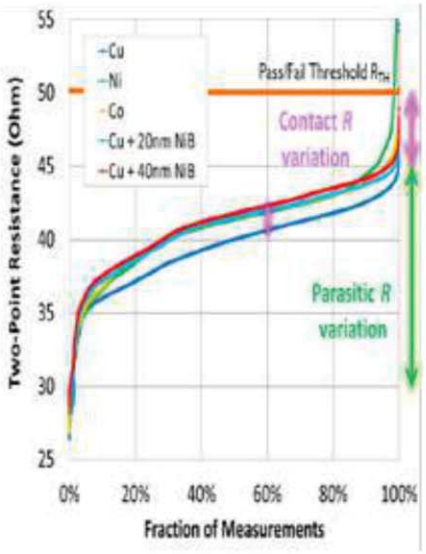

Figure 7: Cumulative distribution function plots of two-point resistance measurements between shorted micro-bumps with varying metallurgies at their probe surface.

Probe marks on Cu micro-bumps are small (see Figure 8a), and therefore, we do not expect a negative impact on the interconnect yield after stacking despite the probe mark. For Cu/Ni/Sn micro-bumps, the probe marks are relatively larger (see Figure 8b) because these micro-bumps are smaller and so the probe tip is relatively big, but mainly because Sn is a much softer material than Cu and easily deformed. Fortunately, Sn is very forgiving when it comes to stacking. Experiments in which we compared all four cases of yes/no probing the bottom/top micro-bumps, followed by stacking did not

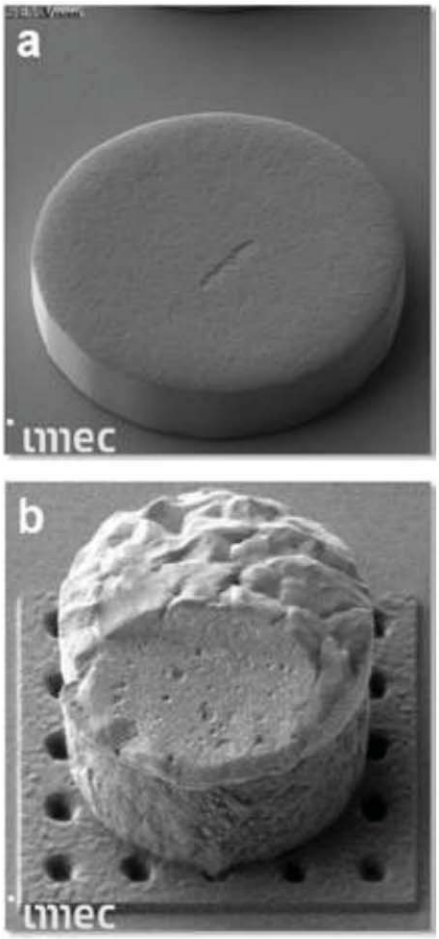

Figure 8: Probe marks on micro-bumps with different dimensions and metallurgies: a) ø25µm Cu micro-bump; and b) ø15µm Cu/Ni/Sn micro-bump.

reveal any impact of probing on the interconnect yield [4]. Optionally, the Sn micro-bumps can be reflowed after probing, to restore the Sn cap, remove the probe mark, and thereby prevent particle entrapment.

The data presented above highlights factors that impact the industry's bottom line concerns. Probe cards are consumables with a limited number of touchdowns. The advanced FormFactor Pyramid Probe® RBI probe cores are not inexpensive, so every touchdown adds cost. However, comparisons with the cost analysis tool 3D-COSTAR from TU Delft and imec [4-6] revealed that using these expensive advanced probe cards to probe on micro-bumps is still significantly cheaper than its alternative: providing a limited number of large, easy-to-probe pre-bond probe pads, as this will increase the test time significantly and still leaves the micro-bumps untested.

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