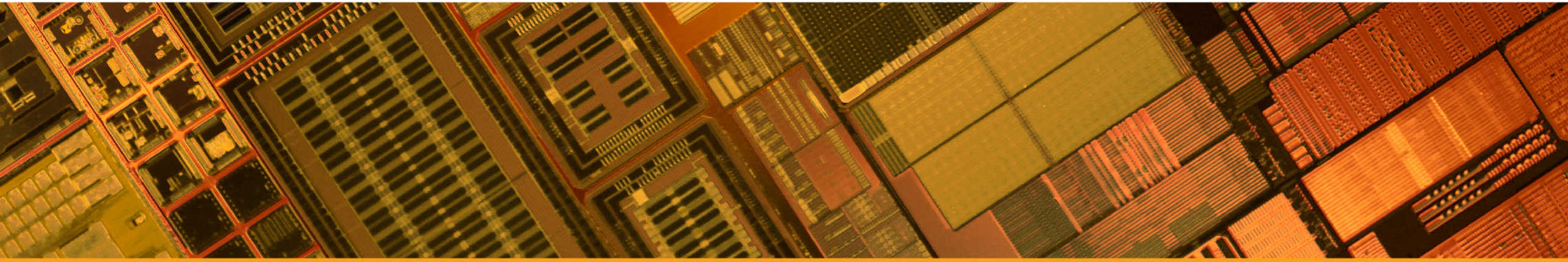
SEMICON® WEST

BEYOND SMART

Advanced Packaging – It's Changing the World of Wafer Test

Mike Slessor, President and CEO
FormFactor, Inc.



FormFactor™

semi

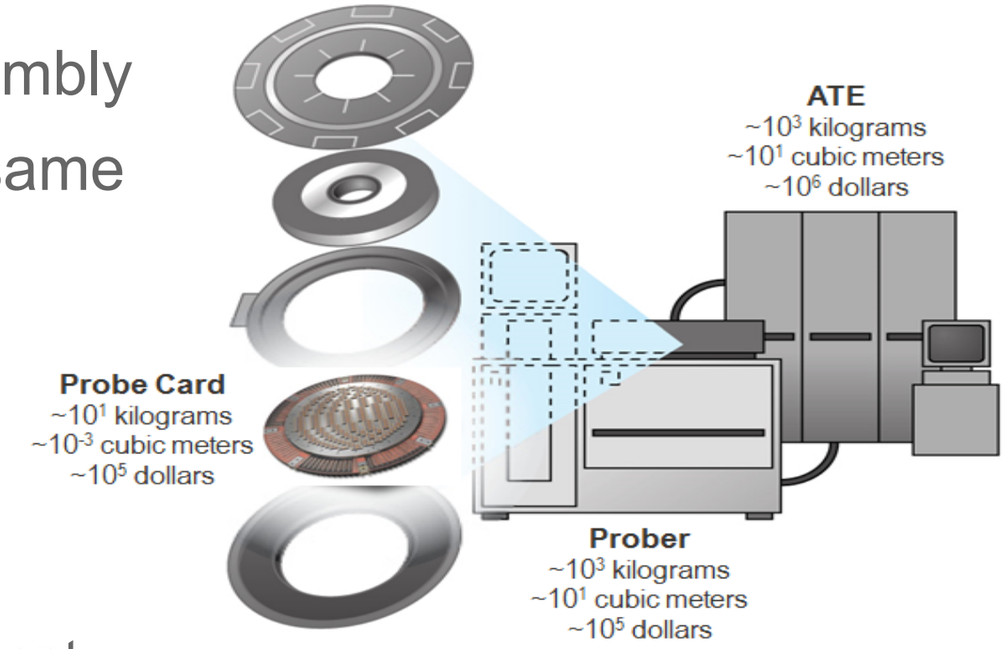
A Roadmap For Our Next Hour Together

- Introductions and level setting
  - Wafer test, FormFactor, and advanced packaging
- Why does advanced packaging have anything to do with wafer test?
  - Or, aren't you test guys just trying to hitch yourself to this trendy bandwagon?
- Advanced packaging examples and implications for wafer/die test
  - Challenges, alternatives, options, and tradeoffs

- Q&A and open discussion

What Is Wafer Test?

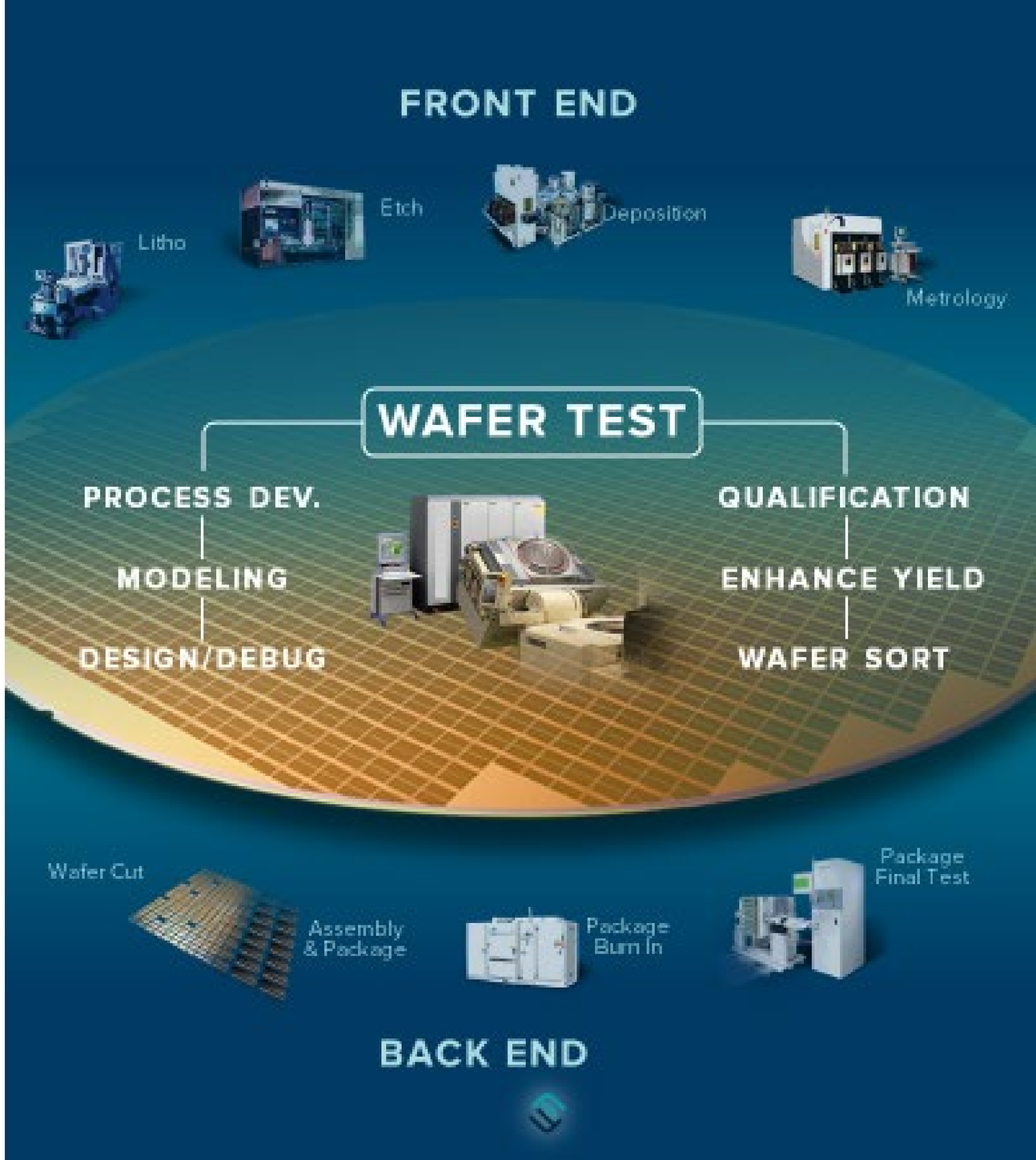
- Electrical test after wafer fab, prior to backend assembly
- DUT(s)-to-ATE connection typically made through same contacts that connect die to package
  - Wirebond pads, flipchip bumps, copper pillars, TSVs, etc.
- Key components of wafer-test cell:
  - ATE: Instruments & power supplies to stimulate and interrogate the DUT(s)
  - Prober: Wafer (die) handling, positioning, and environment
  - Probe card: Device-specific interface providing DUT(s)-to-ATE connection



FormFactor™

A Leader in Electrical Test and Measurement

Accelerating Customer Profitability



FormFactor At a Glance

PROBE CARDS FOR PRODUCTION

50,000,000+ MEMS PROBES/YEAR

PROBE SYSTEMS FOR ENGINEERING

10,000+ INSTALLED PROBERS

NASDAQ

FORM

SINCE 1993

2018 REVENUE

OVER **$500M**

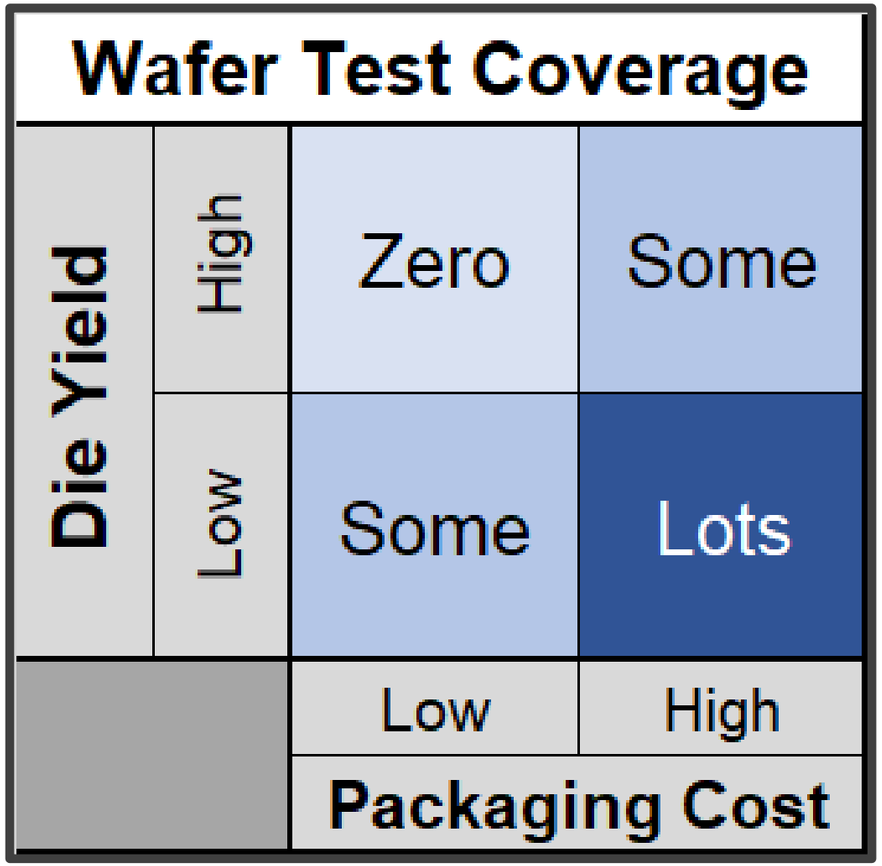
LIVERMORE CALIFORNIA HQ

GLOBAL REACH

1,600 PEOPLE

Why Do Customers Spend $$$ On Wafer Test?

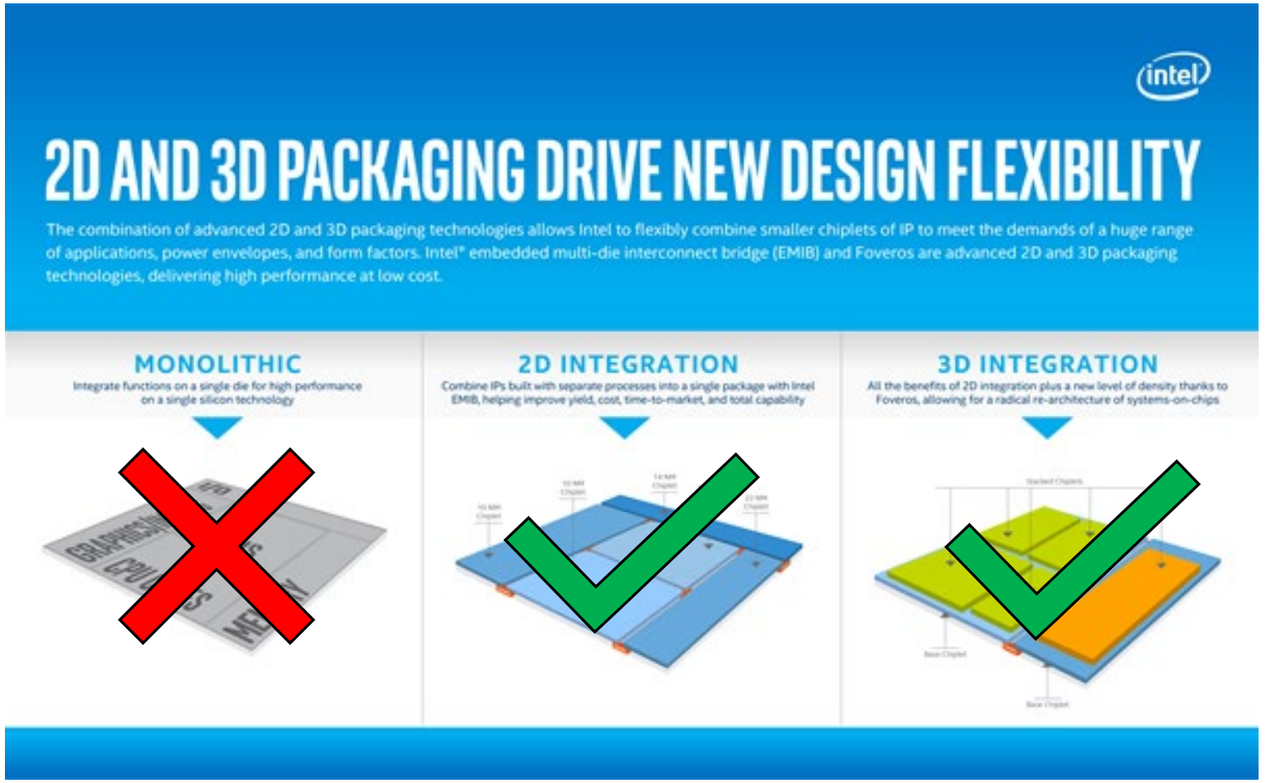
- Avoid wasted cost of packaging a bad die
  - Valuable when yield low and backend cost high
  - Test cost must be << bad-die packaging cost
- Inform an adjustment/trim/change
  - Exercise redundancy (DRAM)
  - Feedback for frontend fab process changes
- As outgoing QC for product title transfer
  - Bare-die sales (or wafer-packaged die)
  - Foundry-fabless-OSAT handoffs



What Do We Mean By “Advanced Packaging”?

System in Package

Source: Taranovich (ASE), EDN 1/4/17



Source: https://newsroom.intel.com/wp-content/uploads/sites/11/2018/12/2d-and-3d-packaging-drive-new-design-flexibility.jpg

Advanced Packaging = Assembly of multiple die either directly to each other or through interfaces with interconnect densities and electrical performance comparable to that of the individual component die

It's Recharging Innovation in the post-Moore's Law Era (& can help cost/yield)

circuit breaker

Intel's 10nm Cannon Lake chips are delayed again

Mass production is expected to start in 2019 now

By Chaim Gartenberg | @cgartenberg | Apr 27, 2018, 12:34pm EDT

COMPONENTS

CES 2019: Moore's Law is dead, says Nvidia's CEO

The long-held notion that the processing power of computers increases exponentially every couple of years has hit its limit, according to Jensen Huang.

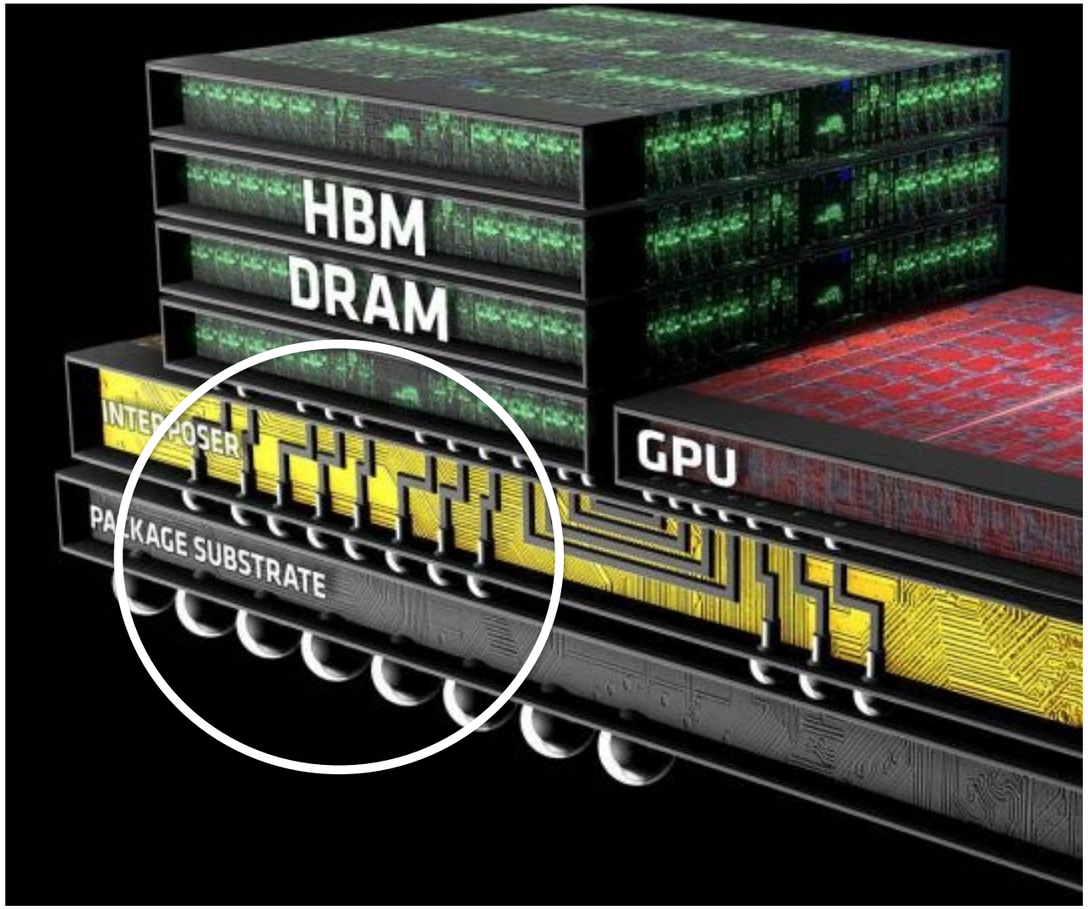
BY SHARA TIBKEN | JANUARY 9, 2019 11:46 AM PST

Source: Su (AMD), IEDM 2017

"Heterogeneous integration of best-in-class technology is a way to continue Moore's law performance trends"

Nagisetty (Intel), IEEE Spectrum April 2019

AMD's Fiji – An Early Commercial Example of Advanced Packaging



Source: https://www.anandtech.com/show/9390/the-amd-radeon-r9-fury-x-review/3

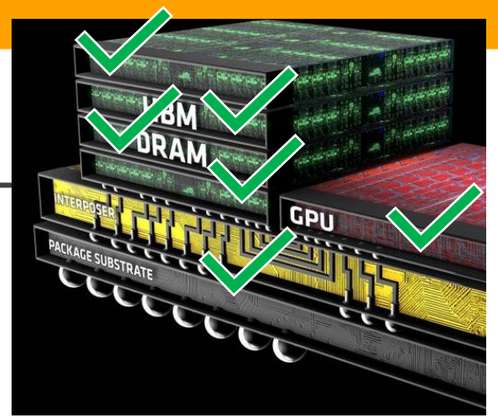
Heterogenous integration of 3 components:

1. Graphics Processing Unit (GPU)
   - Fabbed on 28nm foundry process
2. High Bandwidth Memory (HBM) DRAM
   - Fabbed on 2Ynm DRAM process
   - Four DRAM die stacked on a logic base die
     - A standalone sub-example of advanced packaging
3. Silicon Interposer
   - Fabbed on 65nm foundry BEOL Cu process
   - Density enables wide high-speed memory bus
     - Not possible with an organic substrate

- Connected with ~10k "microbumped" Through-Silicon-Vias (TSVs) at ~50um pitch

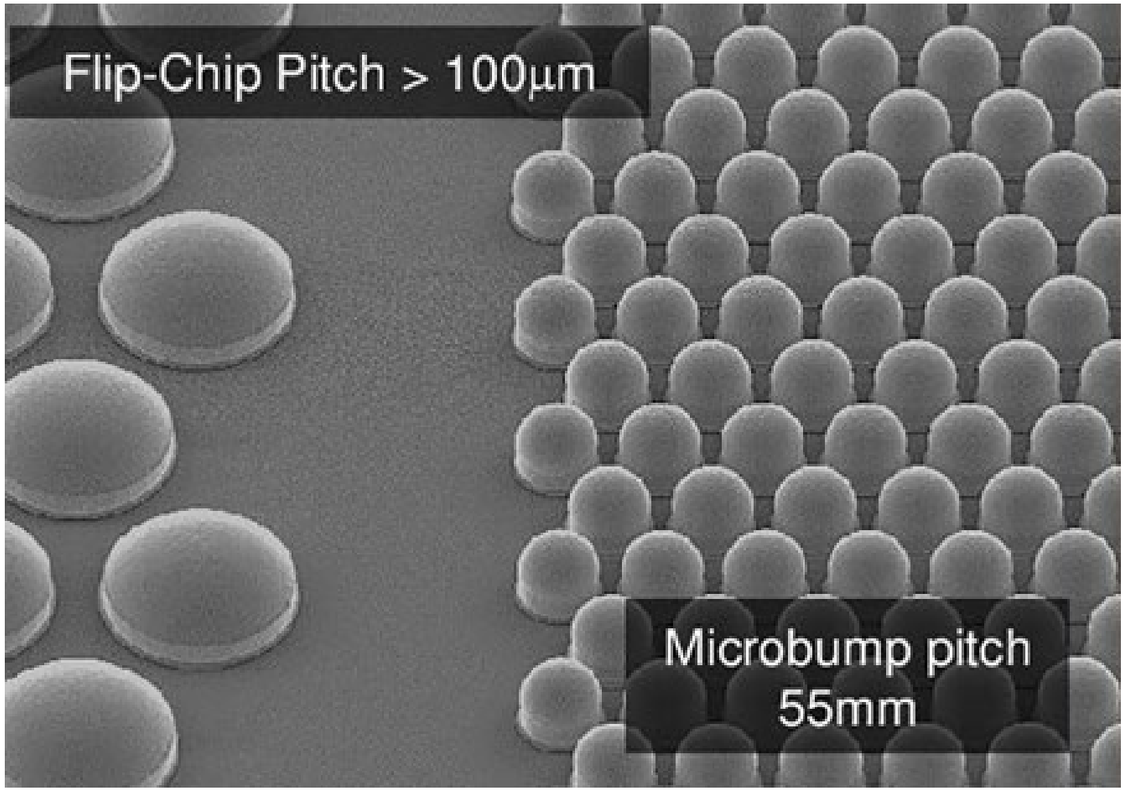
For Test, So What? For One Thing, Coverage

- Ideally, each component is known to be good before integration
  - This has spawned repeated calls for the nirvana of Known Good Die (KGD)
- Caveat #1: "Known Good" within available redundancy/repair
  - Example: Interposers/bridges typically have redundant vias
  - Example: Each HBM DRAM sub-die has significant repairability
- Caveat #2: Economics (always?) dictate something shy of KGD
  - Analogy to our quad chart, fundamentally test is scrap-cost avoidance
  - Final-test and system-test opportunities to prevent escapes
  - Other practical considerations also exist – schedule, risk tolerance, etc.
    - "I thought we had a 90 per cent chance of getting back safely to Earth on that flight but only a 50-50 chance of making a landing on the first attempt", Neil Armstrong
- Cost vs. coverage optimization math is well developed from SiP
  - Though less than Known Good, typically does increase test coverage

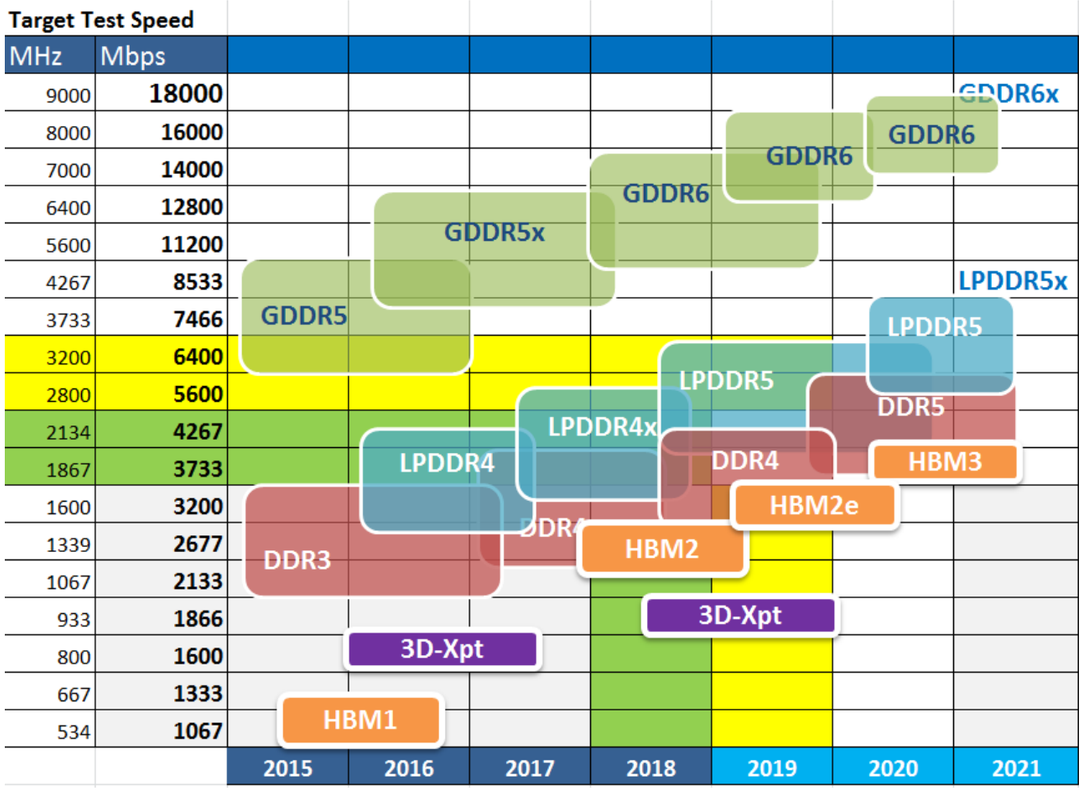


Wafer Test Coverage			
Die Yield	High	Zero	Some
	Low	Some	Lots
		Low	High
		Packaging Cost	

For Test, So What? For Another Thing, Complexity



Source: IEEE Spectrum, April 2019



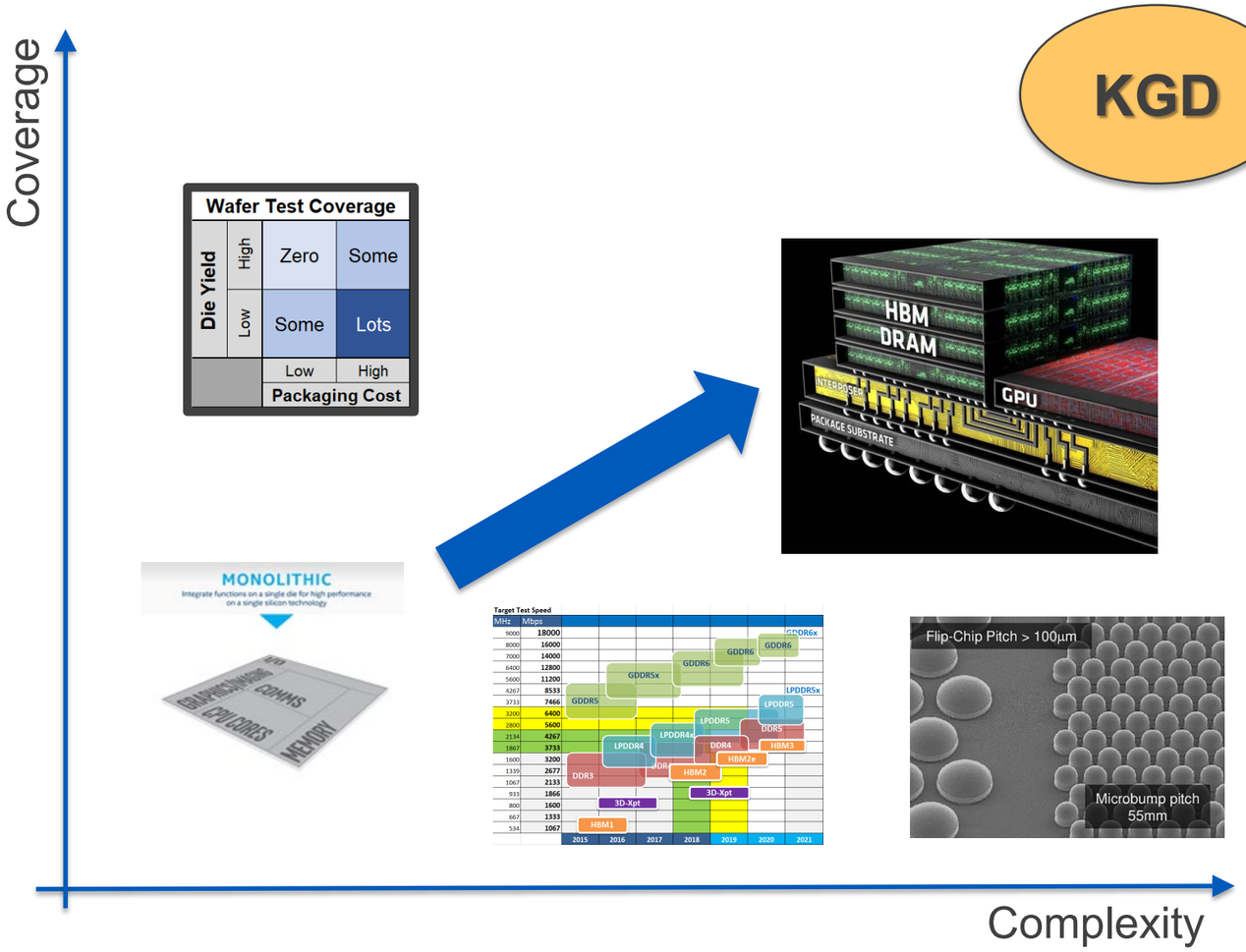
Spatial/Mechanical - Higher Density

- Smaller pitches and higher probecounts
- More delicate contacts made from new materials

Electrical - Higher Performance

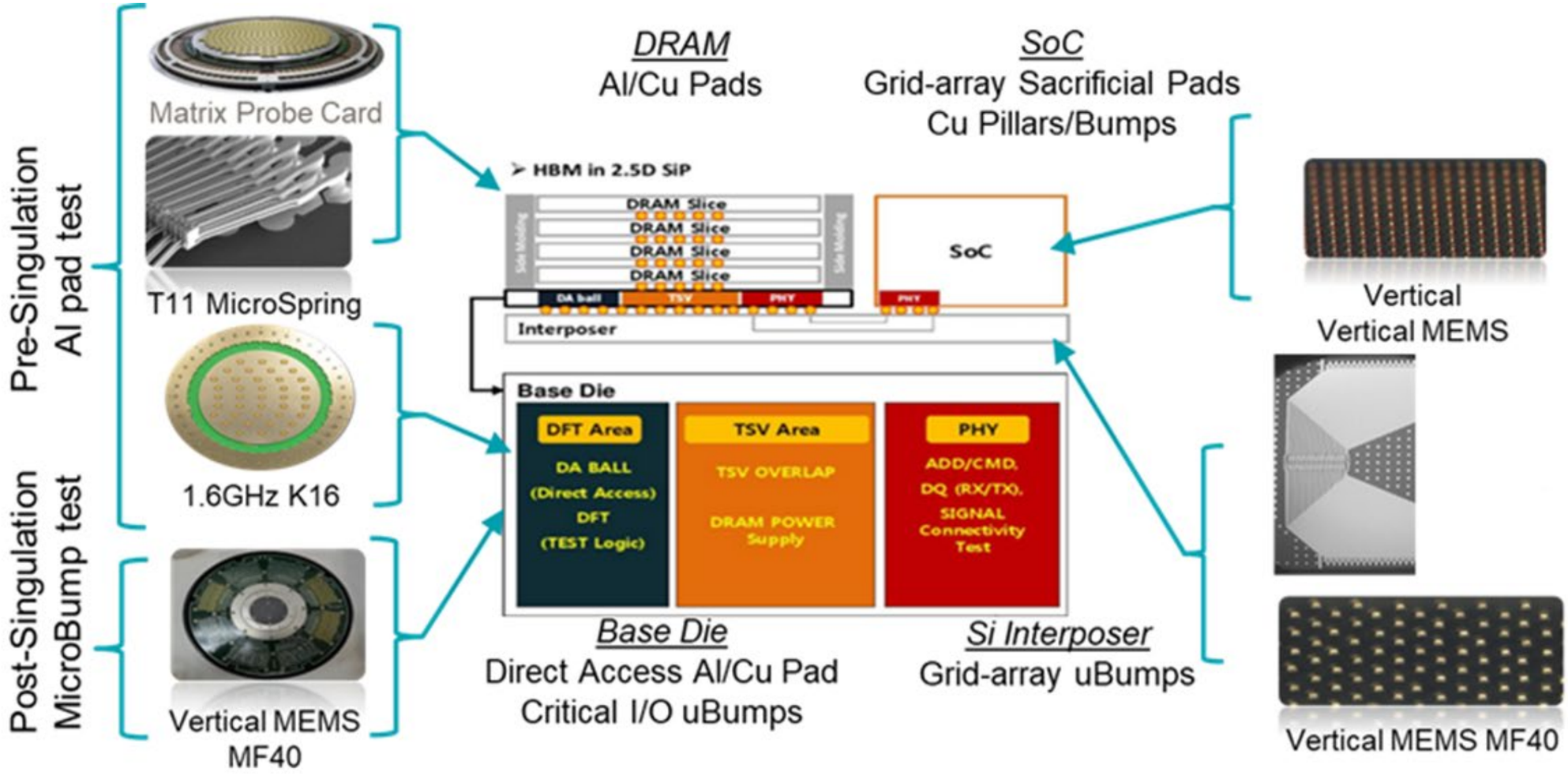
- Higher clock speeds, nearing RF frequencies
- Increased current per contact, much higher power density

Finding A Balance Between Cost, Coverage, and Complexity



- Test cost is a function of both coverage and complexity
- Increasing coverage almost always means increasing test times
  - Lower unit throughput
  - Potential DFT/BIST offsets
- More complexity always means more expensive test cells
  - Novel approaches needed to break scaling, eg, single-die test

There's a Dizzying Array of Possible Test Insertions



Probing Microbumps is Possible, and In Some Cases Rational

2.WIDE-I/O MICRO-BUMP ARRAYS

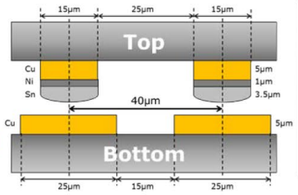
What Do We Want To Probe?

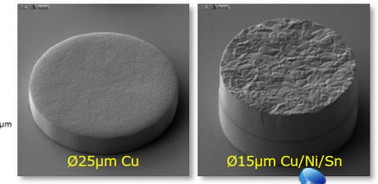
Micro-Bump Probe Targets

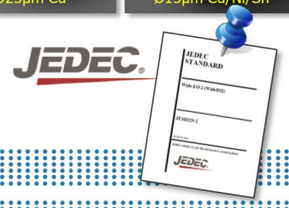
- imec's PoR @40µm pitch
- Today's advanced industry practice

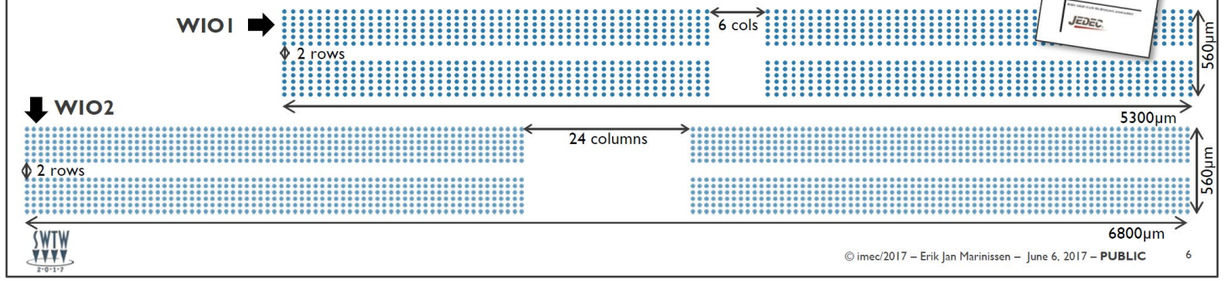
Wide-I/O Micro-Bump Arrays

- WIO1: 1,200 micro-bumps @50/40µm pitch
- WIO2: 1,752 micro-bumps @40/40µm pitch







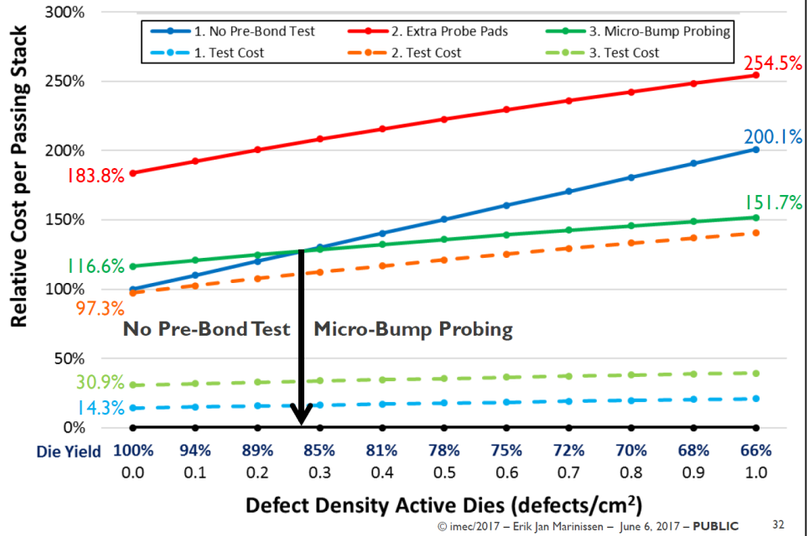


7.TEST COST COMPARISON

3D-COSTAR Cost Modeling Results

1. **No Pre-Bond Test**
   Only acceptable if pre-bond die yield is high
2. **Extra Pre-Bond Pads**
   10× test time increase ⇒ test significant cost-add
3. **Micro-Bump Probing**
   expensive advanced probe card is minor overall cost contributor

No difference in product quality due to Final Test!



Source: Marinissen (IMEC) and Kiesewetter et al (FormFactor), SWTW 2017

- Successful demonstration of viable direct-on-each-microbump probe+test
  - Full 2-D array layouts at ~40um pitch on both solder and copper contacts
  - Reasonable region of defect-density space where this makes economic sense
- Significant current drive limitations in using microbumps as a DUT-test interface

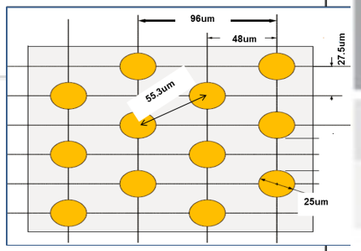
Singulated HBM Die-Level Functional Test Through the Microbumps

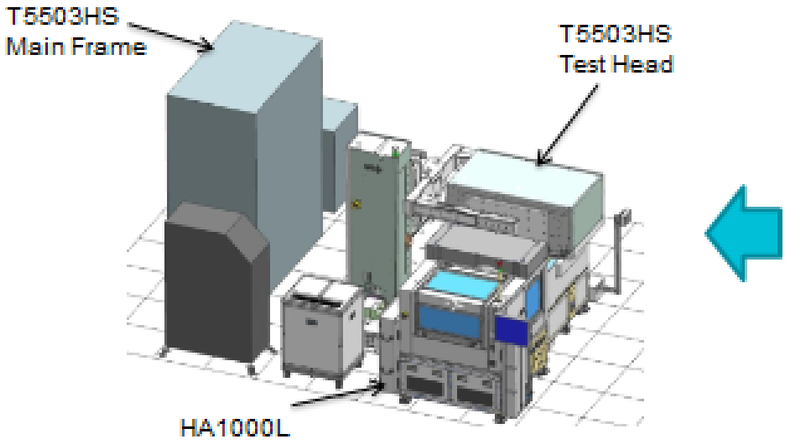
Direct micro-bump probing – Bare Die Handler

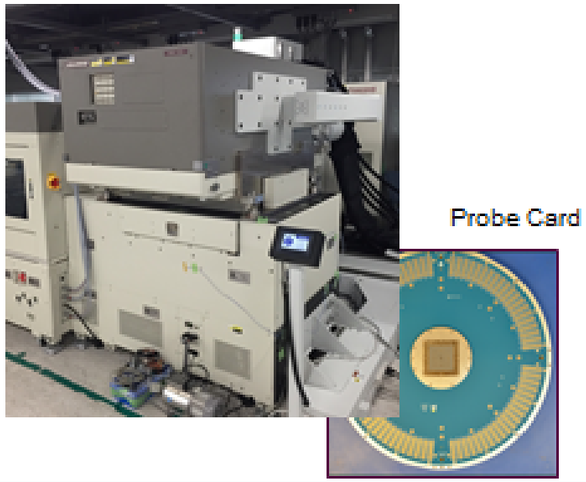
Die Handling & Micro Bump Contact are needed

HBM KGSD Test Solution

- HA1000L : Die Level Handler (Advantest)
- T5503HS : Memory Test System (Advantest)
- Probe Card : Probe Card for HBM (FFI)

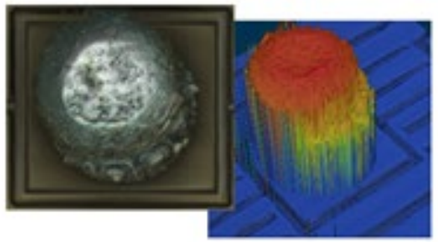


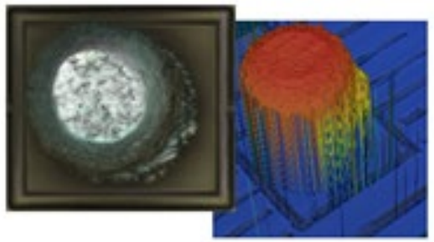


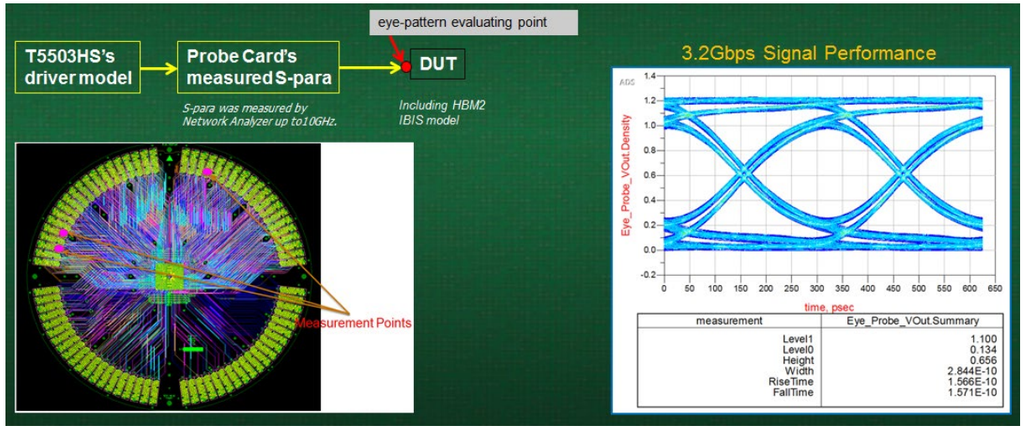


COMPASS 10

Condition	T.T:600sec 1 time	T.T:600sec 2 times
Scrub depth[um]	2.61	2.99
Scrub diameter[um]	14.81	15.04

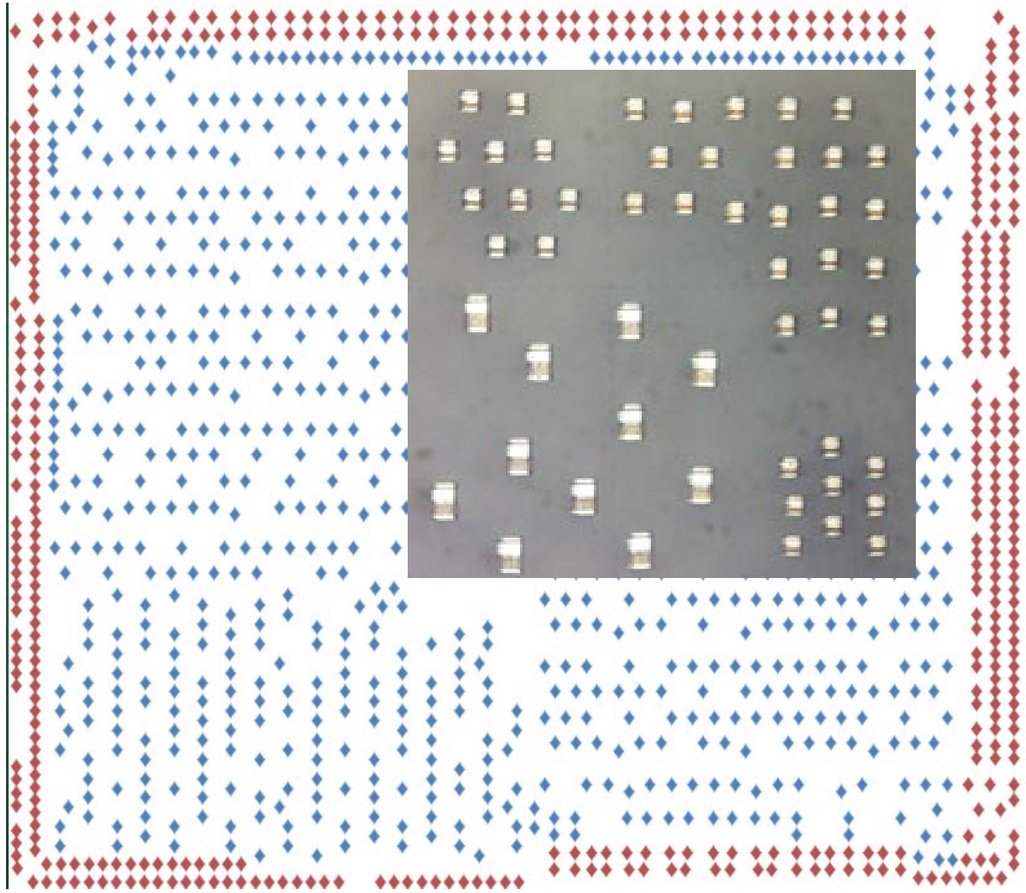






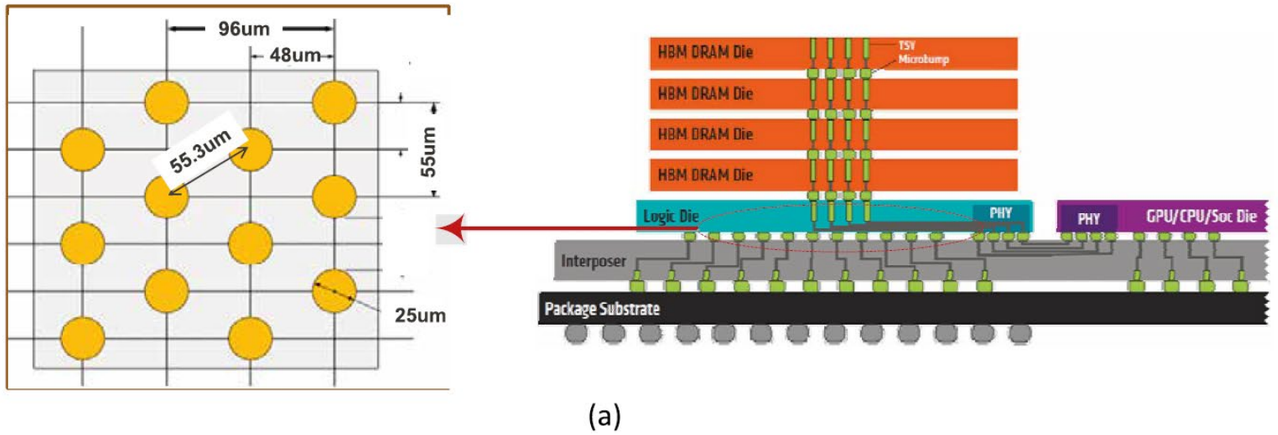
Source: Kiyokawa (Advantest) and Nhin (FormFactor), Compass 2019

Localized In-Die Optimization using Hybrid Probe Arrays



- Approach: Use different probes in different areas of the die to do different jobs
  - Enables decoupling of different requirements
  - Relies on composite metal MEMS technology to match force, wear, etc. between probes
- An example use for application-processor test:
  - I/Os at fine pitch with low current requirements
  - Powers/Grounds at larger pitch with much higher current needs
  - Much higher uptime from reduced probe burn events
  - 40% improvement in power impedance
- Many permutations possible
  - Ex: One probe contacting multiple bumps

And Now for Something Completely Different: HBM with Test Pads



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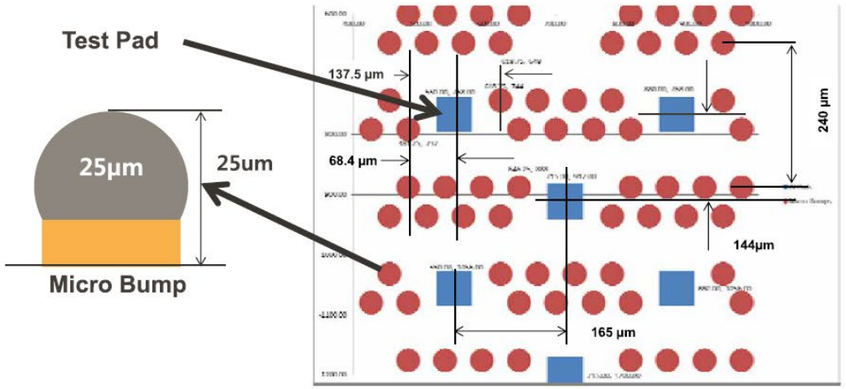

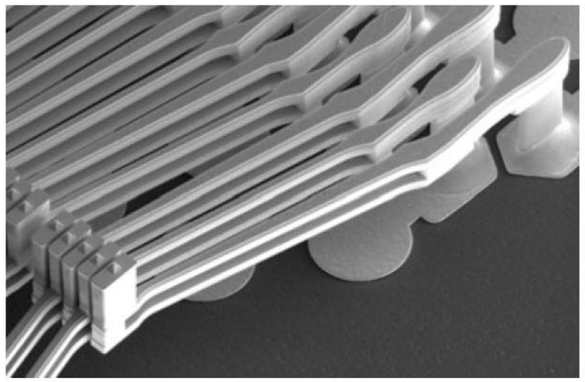

- Approach: Avoid using packaging contacts for test
  - Possible when contact-packing is sparse
- Challenges:
  - Probe design and layout
  - Signal routing for high-speed performance
    - Typically test at DRAM clock speed
- Advantages:
  - No microbump damage
  - Much higher parallelism
  - Similar approach to “regular” DRAM sort

Source: Loranger+Yaglioglu (FormFactor) and Oonk (Teradyne), IEEE Design & Test 2016

Summary and Conclusions

- Advanced packaging will fill the vacuum left by the end of Moore's Law
- But, the burden shifts from the front end to the back end (or middle end)
  - Where lithography and inspection once drove, now assembly and test
- Significant challenges with increasing test complexity and coverage
  - Both technical and economic challenges
  - Complexity: higher densities, faster speeds, etc.
  - Coverage: composite yields of component die
  - KGD is a comforting ideal, but too expensive
- Many options and choices available for optimization
  - Needs multi-supplier and customer collaboration