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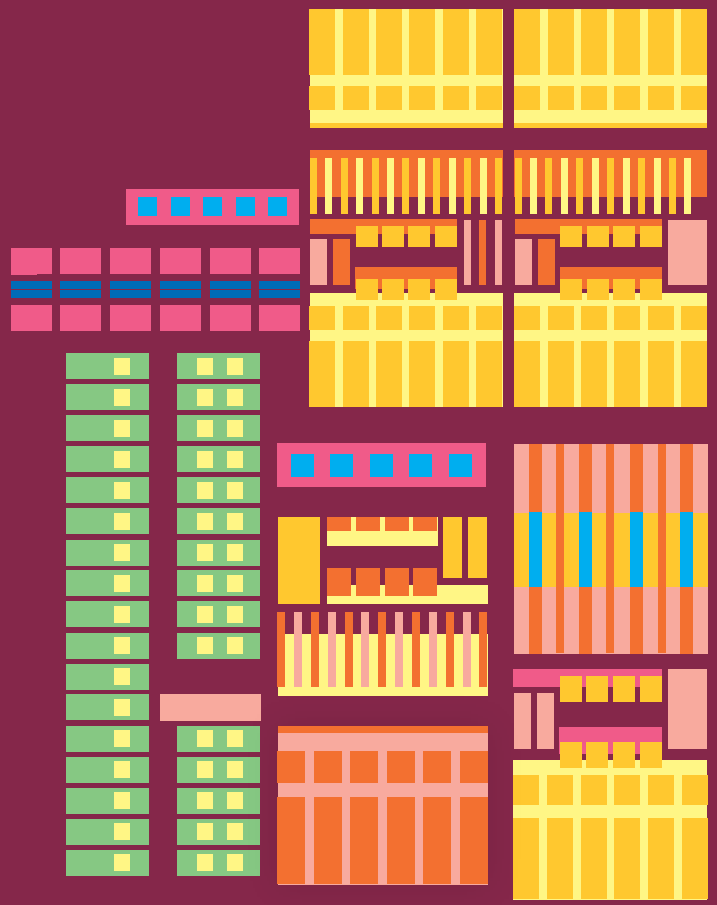
Feb 5-7, 2020 | COEX

semi™

Achieve the balance of test cost, coverage and complexity of Advanced Packages and HBM

Quay Nhin

Product Marketing Manager, FormFactor



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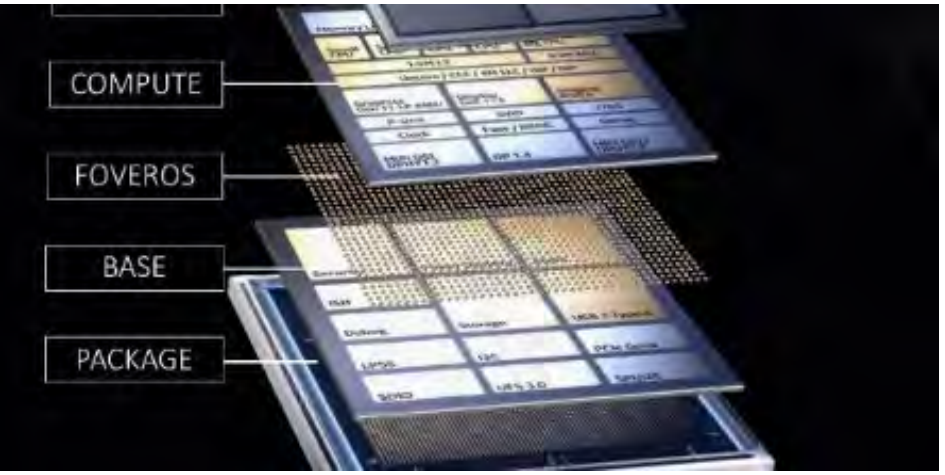
Achieve the balance of test cost, coverage, and complexity of Advanced Packages and HBM

FormFactor Test Solutions Enable the Acceleration of Advanced Packaging

DESIGN THE SMARTER FUTURE

Agenda

- Rapid adaption of Heterogeneous Integration architecture
  - Advanced packaging picks up where Moore’s law left off
  - Bandwidth-hungry applications
- Cost versus quality and reliability considerations
  - Test complexity and coverage
  - Single “killer die” dilemma
- Test solutions available today
  - DFT sacrificial pad probing
  - Direct access on micro-bump probing
  - Precision optical surface profiling
- Q&A



Technology driving the semiconductor industry

AI, AR/VR, IoT, Autonomous, 5G, Cloud

- **Samsung Declares "Age of Experience" at CES 2020**
  - Samsung Consumer Electronics President and CEO H.S. Kim
  - Personal care robot, AI-powered home of the future, and a smart city driven by IoT and 5G
- **"Our lives will be transformed everywhere with this AI revolution, data is truly fueling the economy today"**
  - Sanjay Mehotra, CEO Micron Technology
- **"At Intel, our ambition is to help customers make the most of technology inflections like AI, 5G and the intelligent edge so that together we can enrich lives and shape the world for decades to come."** – Bob Swan, Intel CEO

Advanced Packaging Offers Solution Path in the post-Moore's Law Era to Help Performance & Cost

- Classic approach to improve performance and reduce cost runs out of gas
- Engineers always find new and innovative ways to solve the problem
- Implement new architecture → Wafer to Chiplet

COMPONENTS

CES 2019: Moore's Law is dead, says Nvidia's CEO

The long-held notion that the processing power of computers increases exponentially every couple of years has hit its limit, according to Jensen Huang.

BY SHARA TIBKEN | JANUARY 9, 2019 11:46 AM PST

AI Design Forum 2019 Key Takeaways: Moore's Law Is Dead; Long Live Adaptable Architecture!

xilinx-blog
Xilinx Employee

0 0 2,300 07-11-2019 02:39 PM

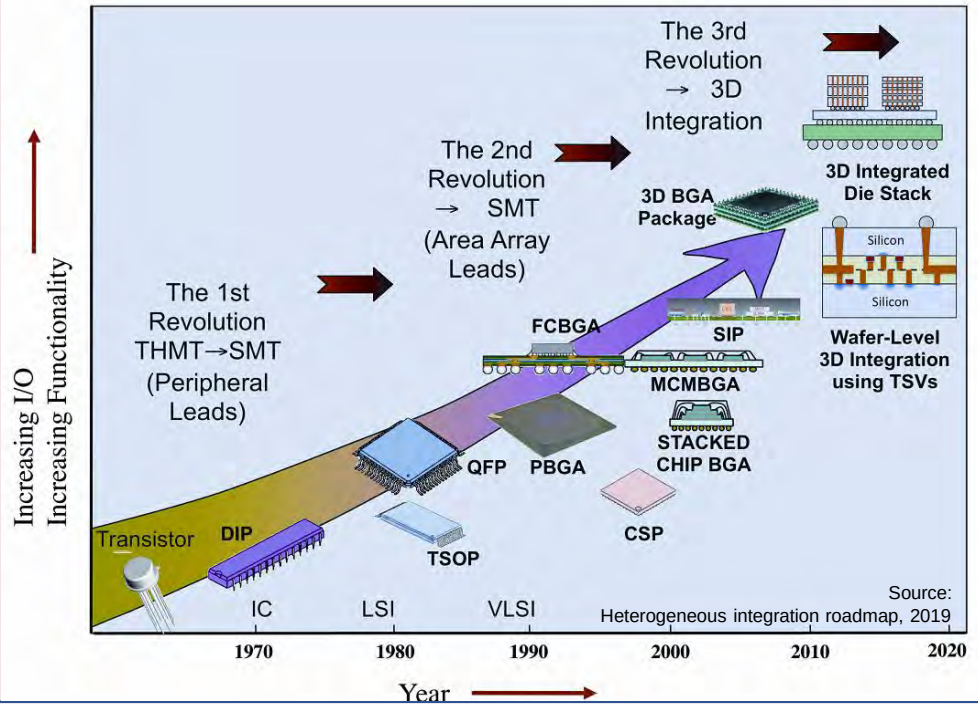
Source: Victor Peng, Xilinx CEO, July 2019 at Semicon West

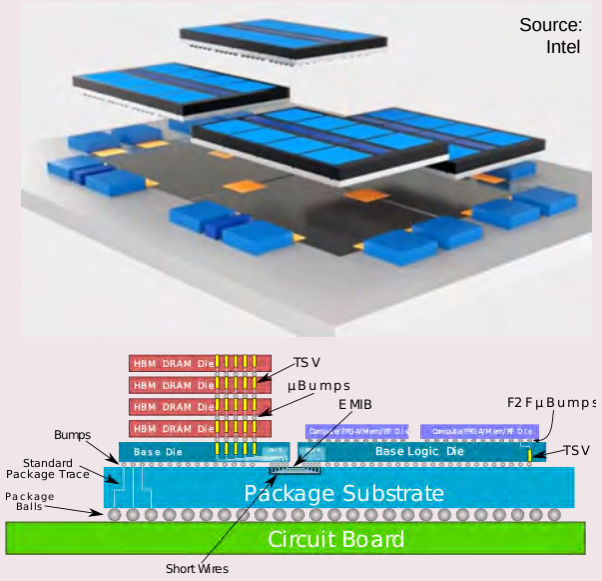
Source: Lisa Su, AMD CEO, July 2019 at Semicon West

Revolution in IC Packaging Technology

- Enable by 2.5/3D Advanced Packaging (According to Yole, it is 40% today, but will cross over the 50% line within the next few years)
- 60 years of innovation in IC packaging
  - "Methods of Making Thru-Connections in Semiconductor Wafers" filed in 1964 and granted in 1967, IBM
  - The first stacked chips fabricated with a TSV process were patented in 1980s Japan, Hitachi & Fujitsu

Single transistor

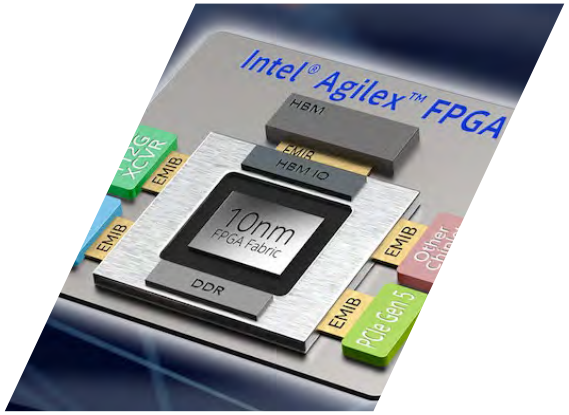


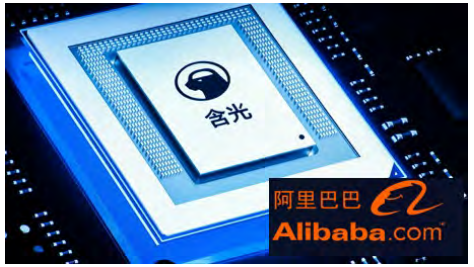


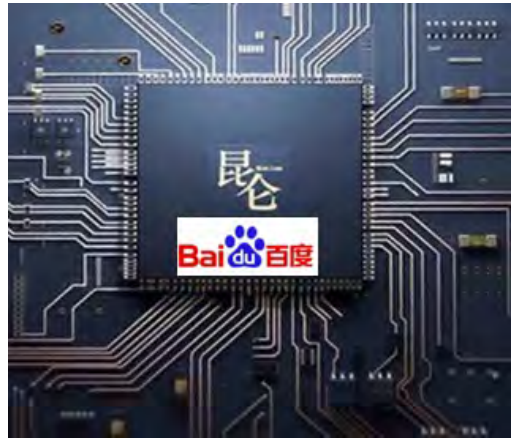
Number of transistors ?

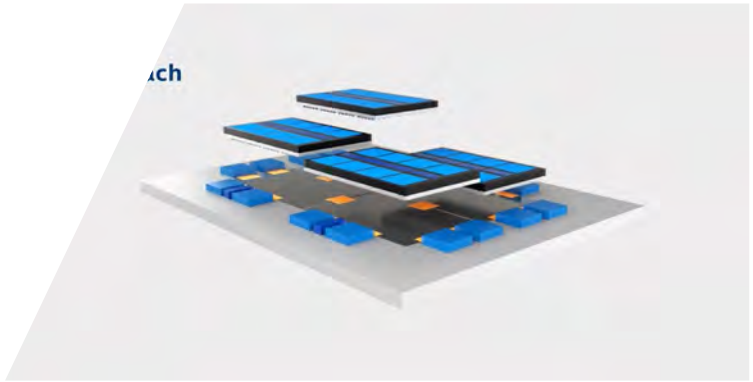
Bandwidth-hungry Applications Accelerating HBM Adoption

A few examples where HBM is used today…..

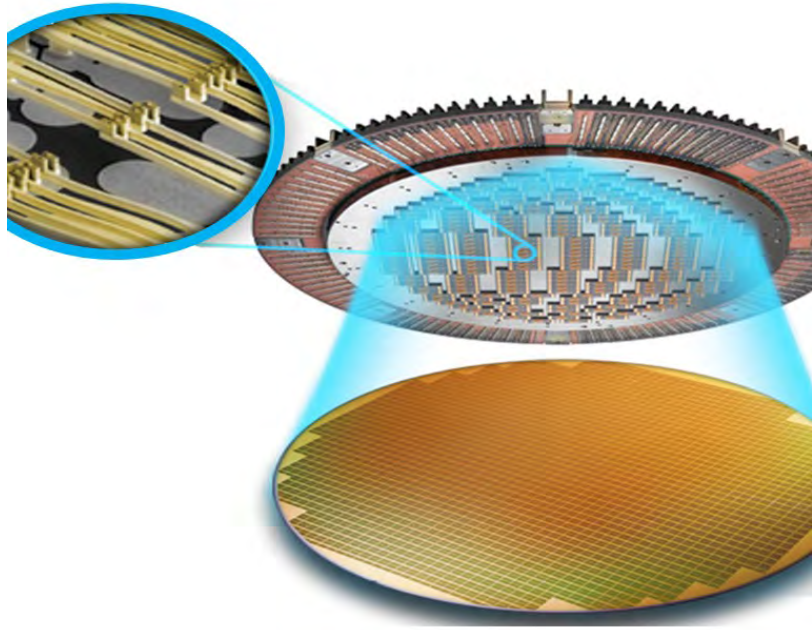








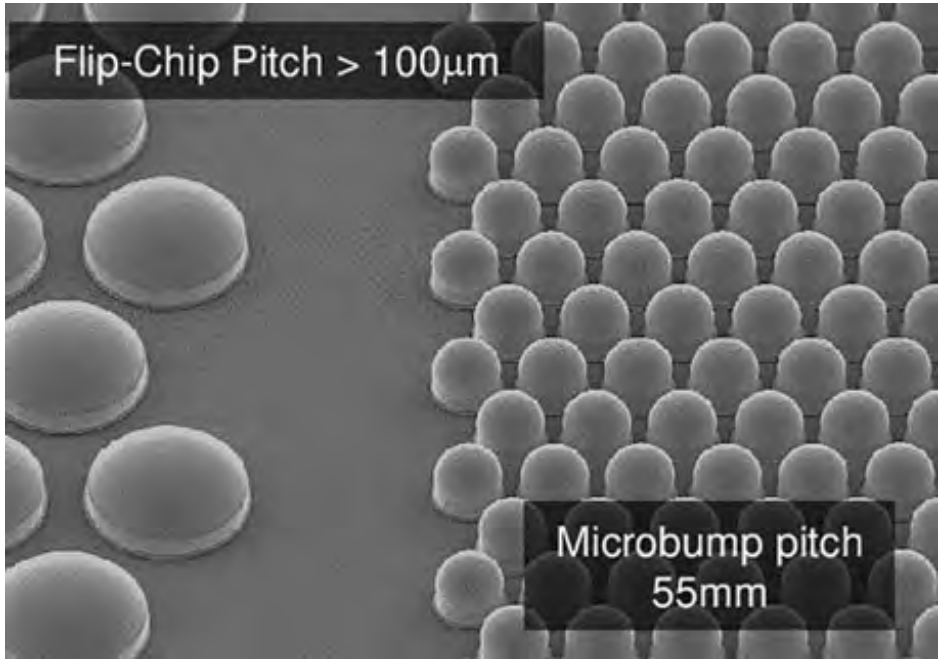
Why Do Customers Spend $$$ On Wafer Test?



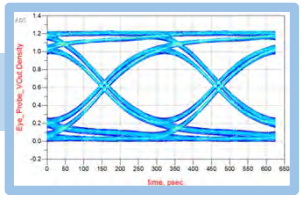
- **Avoid wasted cost of packaging a bad die**
  - Valuable when yield low and backend cost high
  - Test cost must be << bad-die packaging cost
- **Inform an adjustment/trim/change**
  - Exercise redundancy (DRAM)
  - Feedback for frontend fab process changes
- **As outgoing QC for product title transfer**
  - Bare-die sales (or wafer-packaged die)
  - Foundry-fabless-OSAT handoffs

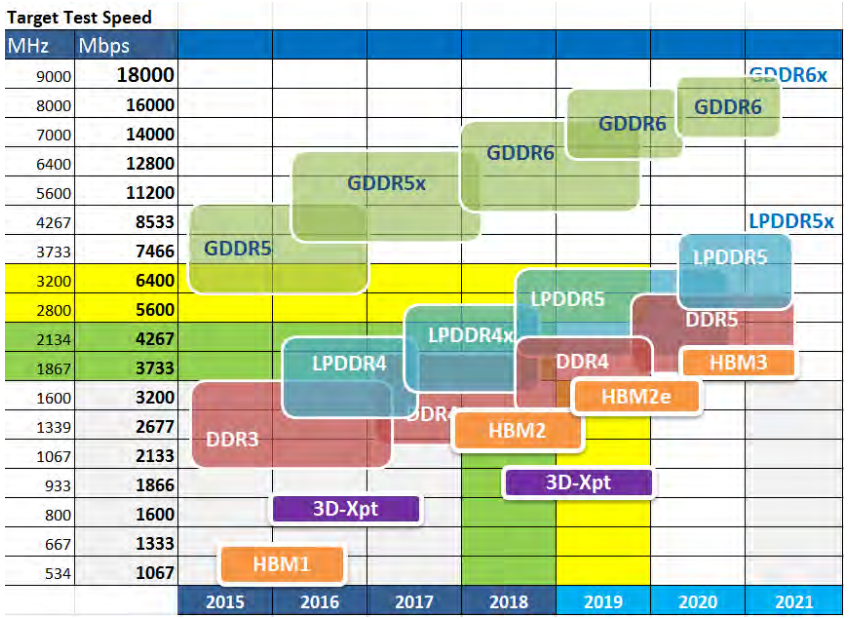
Wafer Test Coverage			
Die Yield	High	Zero	Some
	Low	Some	Lots
		Low	High
		Packaging Cost	

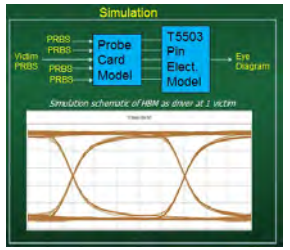
How Does Advanced Packaging Impact Test? Complexity!

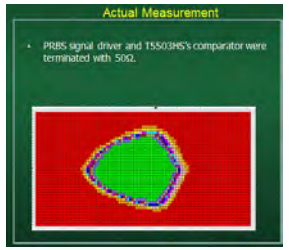


ATE Tester + Probe Card + Wafer =









Spatial/Mechanical – Higher Density

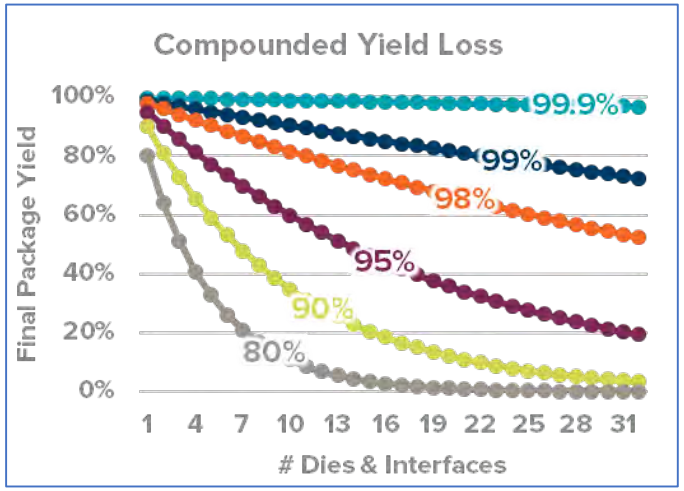
- Smaller pitches and higher probe counts
- More delicate contacts (new materials)

Electrical – Higher Performance

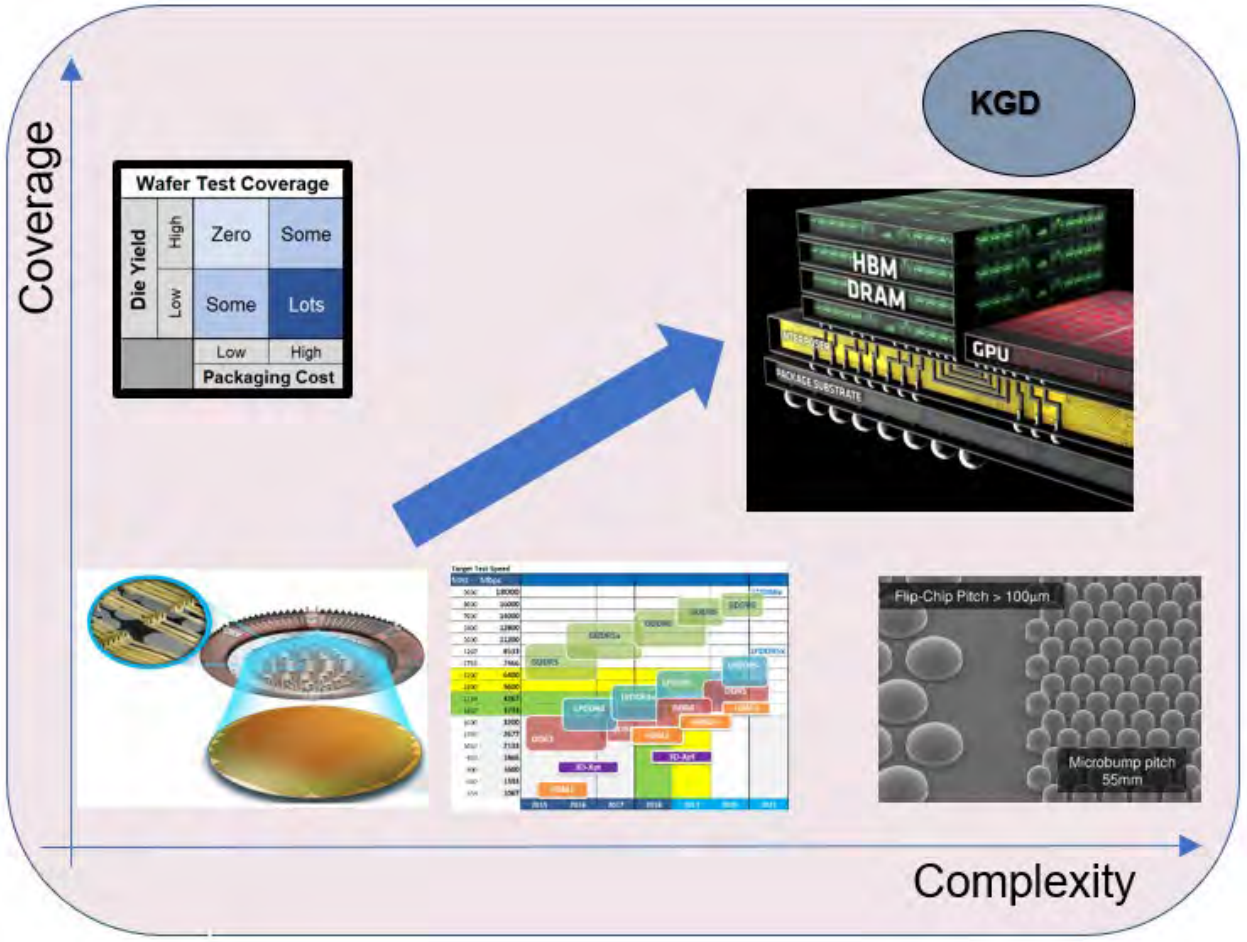
- Higher clock speeds, nearing RF frequencies
- Increased current per contact, higher power density

How Does Advanced Packaging Impact Test? Coverage!

- **Final test of assembled package is necessary, but provides limited insight to improve performance and yield**
- **Ideally, each component is good before integration**
  - Nirvana is Known Good Die (KGD), just test everything
- **Economics dictate something shy of KGD**
  - Pre-package wafer test is fundamentally scrap-cost avoidance
  - Final-test and system-test opportunities prevent escapes
- **Cost vs. coverage optimization comes down to math**
  - Compromise = Probably Good Die (PGD)
  - Hedge bets – e.g., design interposers/ bridges with redundant vias, and build repairability into each HBM sub-die
  - Balance test coverage to catch higher-probability/impact issues, while accepting risk of lesser issues slipping through to final test

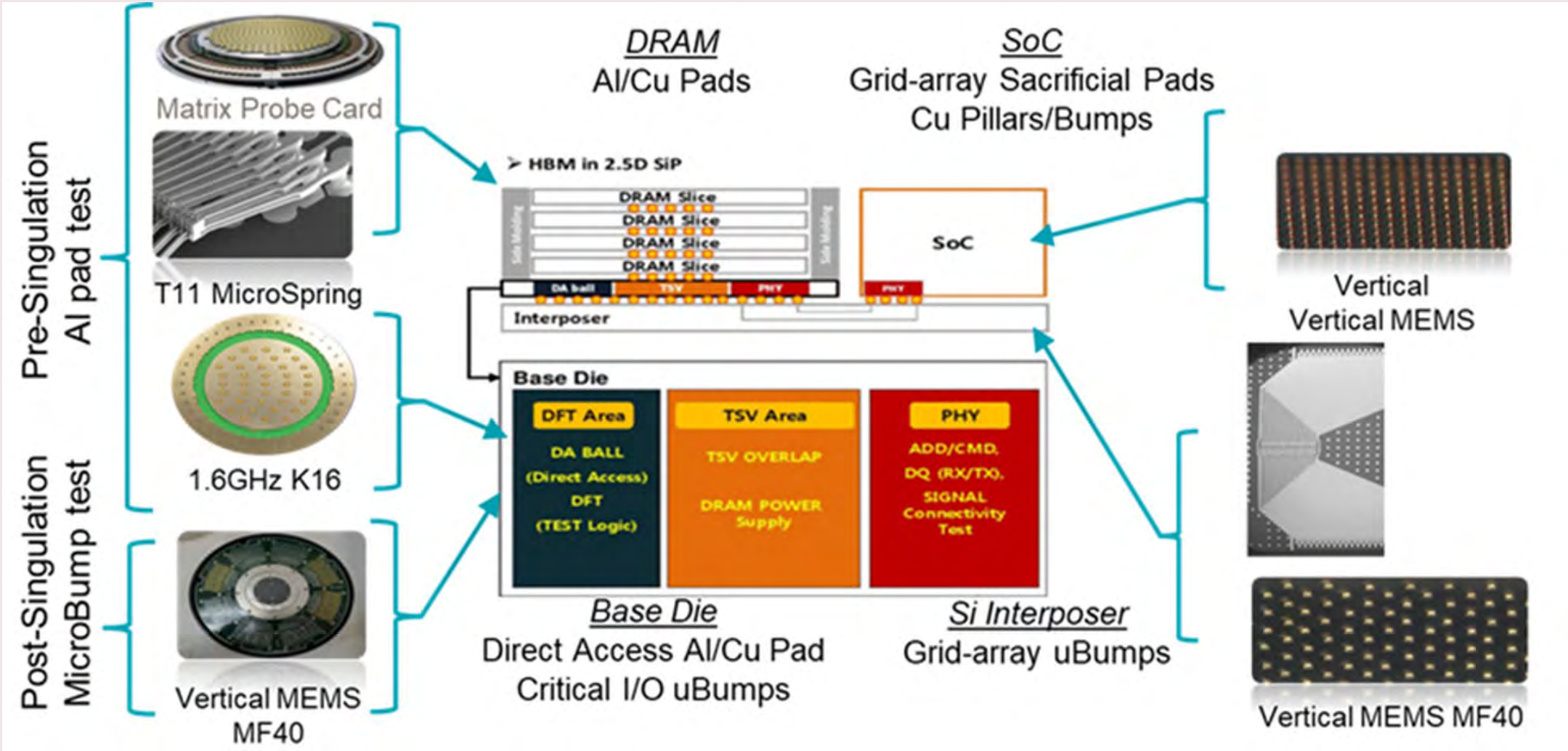


Finding A Balance Between Cost, Complexity, and Coverage

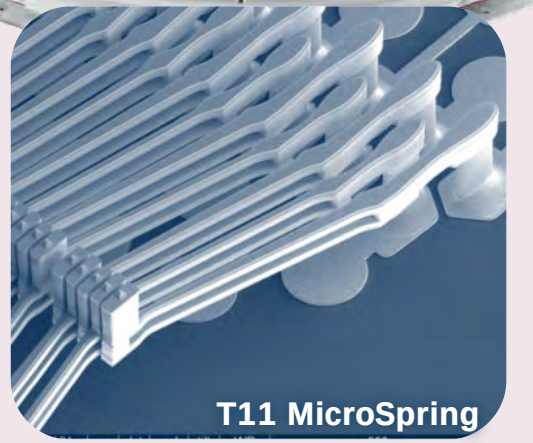


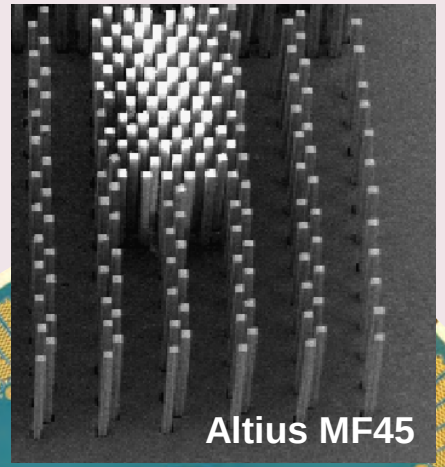
- **Test cost is a function of both coverage and complexity**
- **Increasing coverage almost always means increasing test times**
  - Lower unit throughput
  - Potential DFT/BIST offsets
- **More complexity always means more expensive test cells**
  - Novel approaches needed to break scaling, eg, single-die test

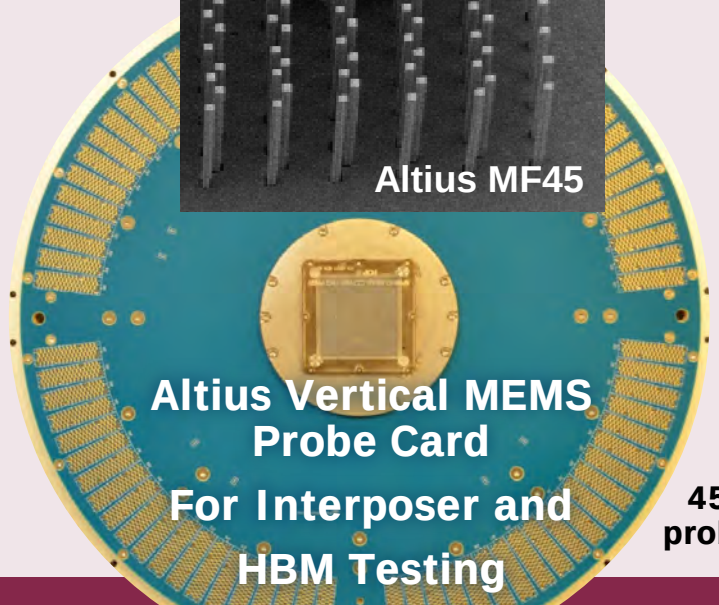
What to Test? So Many Possible Test Insertions…



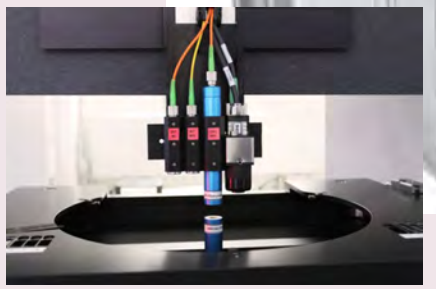
Fortunately, Good Solutions Exist Today



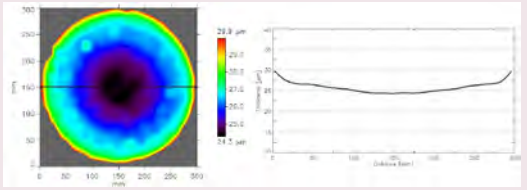




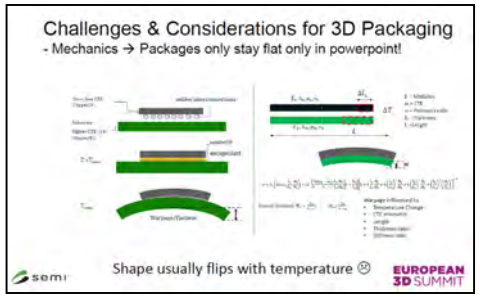
45µm pitch MEMS
probe tip grid array

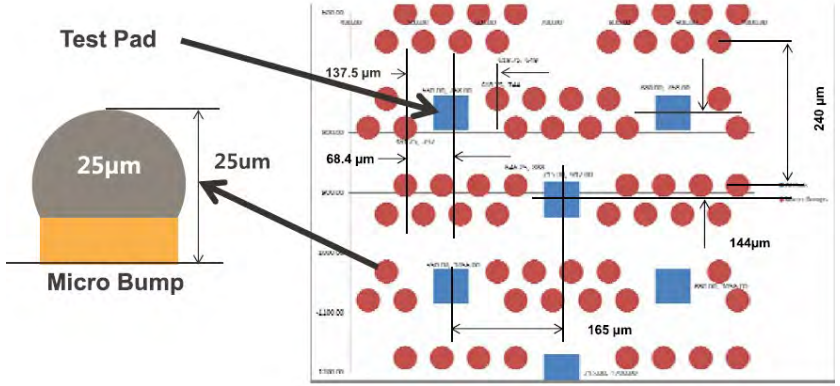


MicroProf® FE/AP



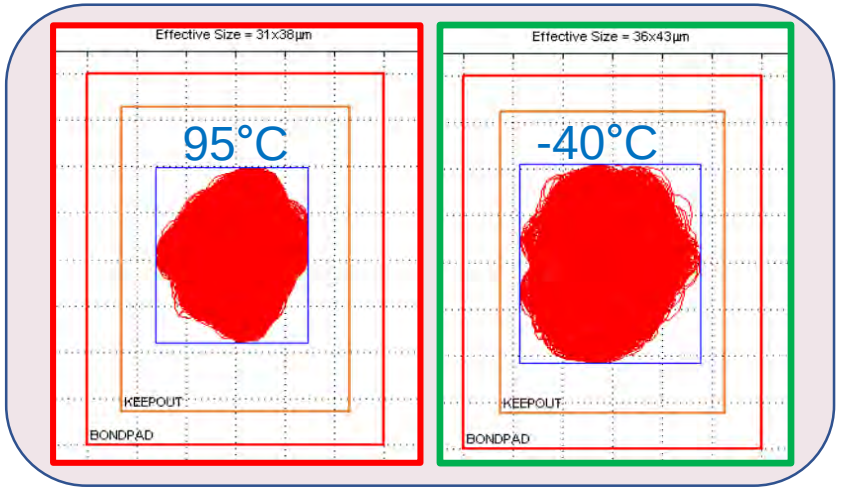
Example
Pad Probing Solution Today



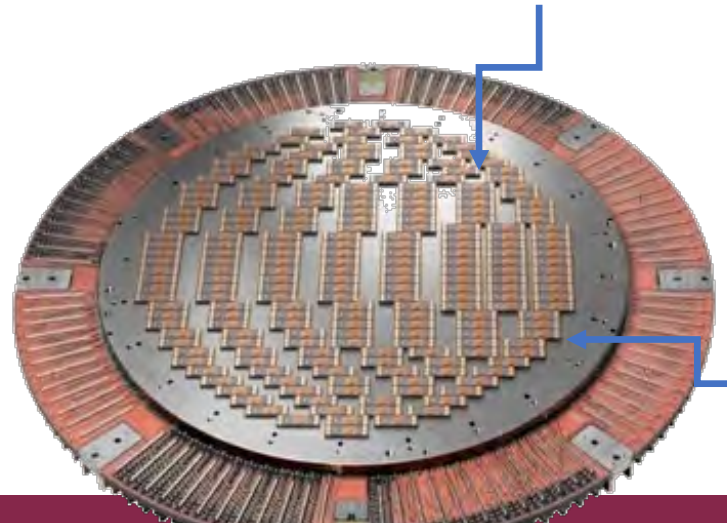


- **Pre-singulated or post singlulated test via sacrificial pads**
  - Base logic die, DRAM core die, KGSD stacked HBM die
  - Test at native HBM operating speed
- **Challenges:**
  - Probe design and layout
  - Signal routing for high-speed performance
  - HBM stacked wafer thermal expansion and warpage
- **Advantages:**
  - Avoid micro-bump damage
  - Much higher parallelism
  - Single temperature or dual temperature probe card capability

Excellent scrub performance and accuracy

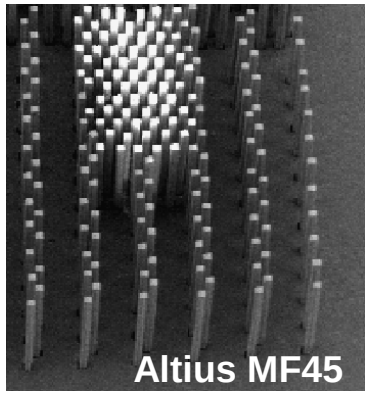


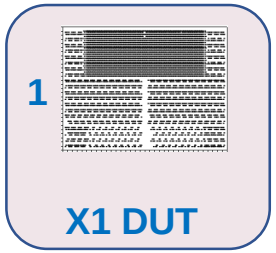
DUTLet attach position scaling

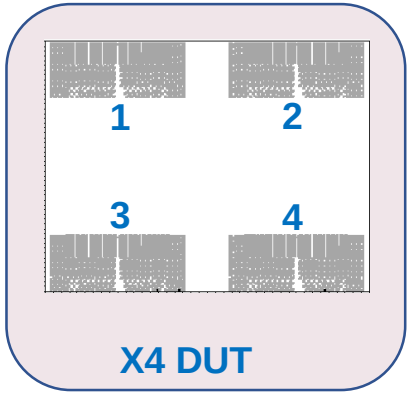


Flexible wafer side stiffener
Able to select a material with desired CTE

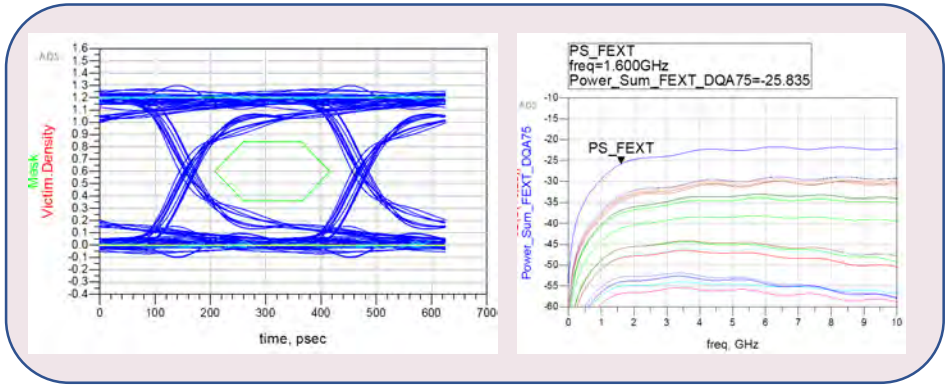
Example
µ-bump Probing Solution Today



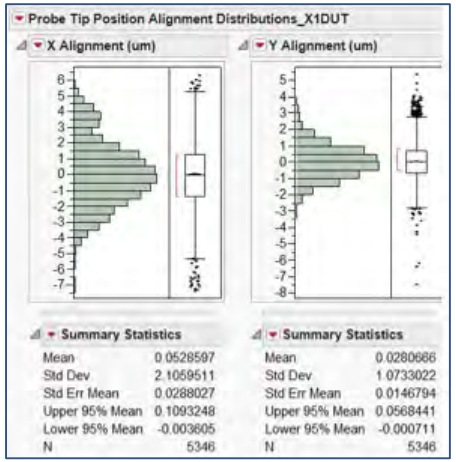




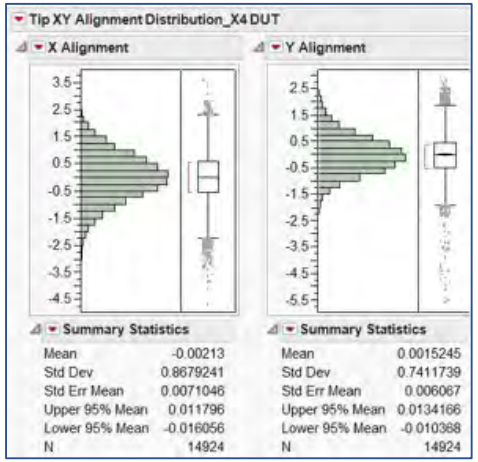
SI/PI target critical: data-eye, PDN, cross-talk



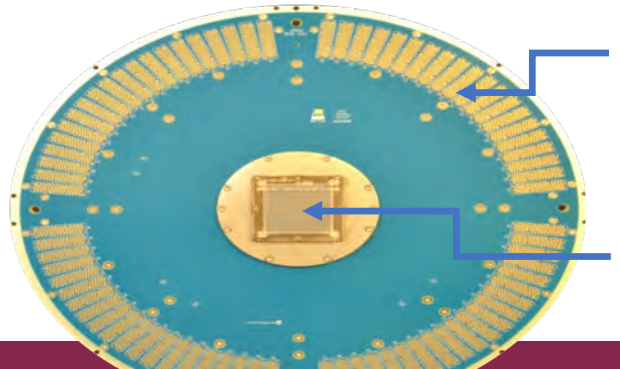
X1 DUT, >5k-pin
<±7.5um XY-err



X4 DUT, ~15k-pin
<±7.5um XY-err



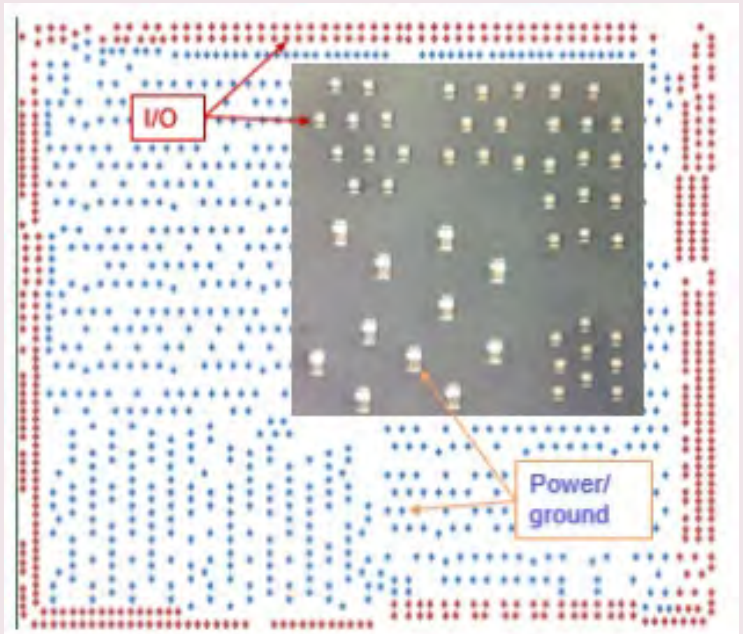
- **Pre/Post-singulated die test**
  - Test at native HBM operating speed
- **Challenges:**
  - Probe design and layout
  - Fan-out on MLO at sub-50um pitch
  - High speed routing meets target SI and PI requirement
- **Advantages:**
  - Probing directly on micro-bump
  - Test result resemble final device performance data
  - Capable of dual temperature



PCB and MLO Designs supports 1.6GHz/3.2Gbps

45um true pitch Probe layout

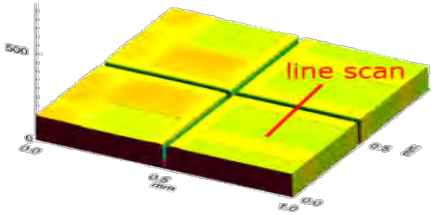
Example –
In-Die µBump Optimization using Hybrid Probes

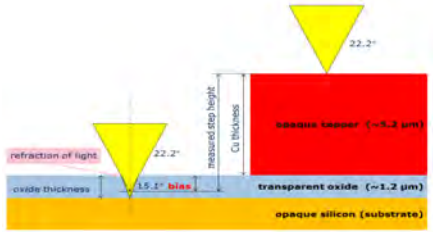


- **Approach: Use different probes in different areas of the die to do different jobs**
  - Enables decoupling of different requirements
  - Relies on composite metal MEMS technology to match force, wear, etc. between probes
- **An example use for application-processor test:**
  - I/Os at fine pitch with low current requirements
  - Powers/Grounds at larger pitch with much higher current needs
  - Higher uptime from reduced probe burn events
  - 40% improvement in power impedance
- **Many permutations possible**
  - Ex: One probe contacting multiple bumps

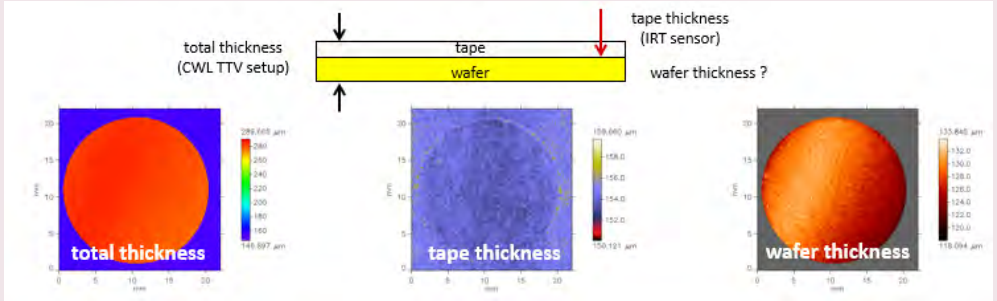
Example –
Sub-micron stacked die or wafer features optical measurement

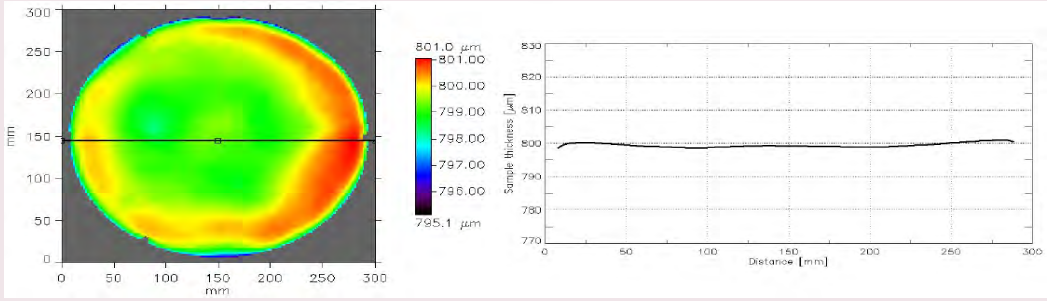
MicroProf® FE/AP





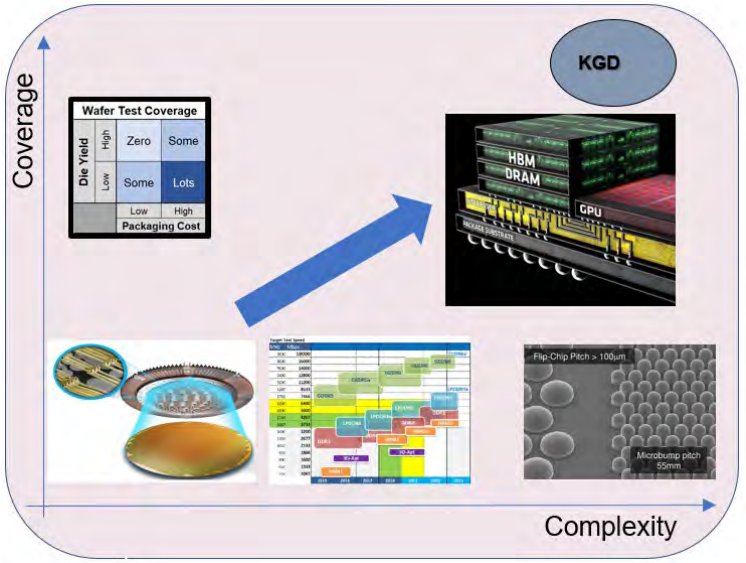
- Fully automated systems with flexible sample handling
  - Trench depth measurements
  - Photo resist thickness or cavity uniformity
  - Temporary wafer or carrier bonding wafer thickness profiling
  - 200mm / 300mm wafer stage
  - Fast and accurate
  - High repeatability and reproducibility





Summary and Conclusions

- Advanced packaging will fill the vacuum left by the end of Moore's Law
- But, the burden shifts from the front end to the back end (or middle end)
  - Where lithography and inspection once drove, now assembly and test
- Significant challenges with increasing test complexity and coverage
  - Both technical and economic challenges
  - Complexity: higher densities, faster speeds, etc.
  - Coverage: composite yields of component die
  - KGD is a comforting ideal, but too expensive
- Many options and choices available for optimization
  - Needs multi-supplier and customer collaboration



Thank You!